



# Efficient Synchronous Step-Up Converter with a 2.7A Switch

## **1 FEATURES**

- Input Voltage Range: 2.2V to 5.5V
- Up to 90% Efficiency at Typical Operating . Conditions
- Quiescent Current: 20µA (TYP) •
- Less than 1µA Shutdown Current .
- Adjustable Output Voltage Up to 5.5V .
- Power-Save Mode for Improved **Efficiency at Low Output Power**
- Low Reverse Leakage Current when VOUT > VIN
- Load Disconnect During Shutdown
- **Output Short Circuit Protection** •
- **Thermal Shutdown Protection** •
- Internal 1.5ms Soft Start Time
- **Operating Temperature Range: -40°C to** +85°C
- **Micro SIZE PACKAGE: TSOT23-6**

### 2 APPLICATIONS

- **Portable Audio Players**
- **Single-Cell Li-Ion Powered Products**
- **Cellular Phones**
- **Personal Medical Products**

### **3 DESCRIPTIONS**

The RS6651 is an internally compensated, 1.1MHz switching frequency, current mode, synchronous step-up switching regulator, which can generate 5V output at 1A load current from a 3.3V rail.

This device turns into power-saving mode to maintain high efficiency by lowering switching frequency. With its antiringing circuitry damping the charge in parasitic capacitor, it reduces EMI interference significantly. Its output is disconnected by the rectifier circuit during shutdown, with no input to output leakage.

RS6651-ADJ is output voltage programmable with an external resistor divider. When the RS6651 is in shutdown mode, the isolation switch disconnects the output from input to minimize the leakage current. The RS6651 also implements output short circuit protection, output overvoltage protection, and thermal shutdown.

The RS6651 is available in Green TSOT23-6 package. It operates over an ambient temperature range of -40°C to +85°C.

#### **Device Information**<sup>(1)</sup>

F	PART NUMBER	PACKAGE	BODY SIZE(NOM)							
	RS6651	TSOT23-6	2.92mm×1.60mm							
(1)	) For all available packages see the orderable addendum at the end o									

lendum at the end of the data sheet.



## **4 TYPICAL APPLICATION**



## **Table of Contents**

1 FEATURES	
2 APPLICATIONS	1
3 DESCRIPTIONS	1
4 TYPICAL APPLICATION	1
5 Revision History	3
6 PACKAGE/ORDERING INFORMATION (1)	4
7 Pin Configuration and Functions	5
8 SPECIFICATIONS	6
8.1 Absolute Maximum Ratings	6
8.2 ESD Ratings	6
8.3 Recommended Operating Conditions	6
8.4 ELECTRICAL CHARACTERISTICS	7
8.5 TYPICAL CHARACTERISTICS	8
9 Detailed Description	
9.1 Overview	
9.2 Functional Block Diagram	
10 TYPICAL APPLICATION CIRCUITS	
11 Application and Implementation	
11.1 APPLICATION INFORMATION	
11.2 Adjustable Output Voltage Version	
11.3 Inductor Selection	
11.4 Selecting the Input Capacitor	
11.5 Selecting the Output Capacitors	
11.6 Layout Guidelines	
12 PACKAGE OUTLINE DIMENSIONS	
13 TAPE AND REEL INFORMATION	



# **5 Revision History**

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2021/11/02	Initial version completed
A.1	2022/04/01	<ol> <li>Update Package Qty on Page 4@RevA.0</li> <li>IsT parameter(TYP) change to 550mA</li> </ol>
A.2	2022/04/18	Add the maximum and minimum values of ELECTRICAL CHARACTERISTICS
A.3	2024/04/09	1. Add MSL on Page 4@RevA.2 2. Update PACKAGE note
A.4	2024/05/29	Update Input Voltage Range: 2.2V to 5.5V



# 6 PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING <sup>(2)</sup>	MSL <sup>(3)</sup>	PACKAGE OPTION
RS6651	RS6651YTH	-40°C ~+85°C	TSOT23-6	6651	MSL3	Tape and Reel, 3000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.



# 7 Pin Configuration and Functions



#### **PIN DESCRIPTION**

	PIN	I/O <sup>(1)</sup>					
NAME	TSOT23-6	1/0/	FUNCTION				
SW	1	I	Boost Switch Node. Connect this node to one terminal of power inductor.				
GND	2	_	Ground.				
EN	EN 3 I		Enable input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.				
FB	4	Ι	Voltage feedback of adjustable output voltage.				
VOUT	5	0	Boost Converter Output. Place a storage capacitor close to this pin.				
VCC	6	I	Supply voltage.				

(1) I = Input, O = Output.



### 8 SPECIFICATIONS

#### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

			MIN	MAX	UNIT
VIN	Input voltage on VCC, VOUT, SW, FB, EN	l	-0.3	6	V
ALθ	Package thermal impedance (4)	TSOT23-6		190	°C/W
τ	Operating Junction temperature <sup>(5)</sup>		-40	150	°C
T <sub>stg</sub>	Storage temperature range		-60	150	°C
	Lead Temperature (Soldering, 10s)			260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) Internal thermal shutdown circuitry protects the device from permanent damage. The actual chip output current is subject to the inputoutput voltage difference, ambient temperature and PCB heat dissipation design.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is PD = ( $T_{J(MAX)} - T_A$ ) /  $R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PCB.

### 8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
Maria		Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
V (ESD)	V <sub>(ESD)</sub> Electrostatic discharge Human-Body Model (HBM), per ANSI/ESDA/JED Charged-Device Model (CDM), per ANSI/ESDA/J		±1200	v

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.



### **ESD SENSITIVITY CAUTION**

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### **8.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Vcc	Input supply voltage on VCC	2.2	5.5	V
V <sub>IN</sub>	Input supply voltage on SW, OUT, FB, EN	-0.3	5.5	V
TA	Operating temperature	-40	+85	°C



# **8.4 ELECTRICAL CHARACTERISTICS**

 $(V_{IN} = 3.6V, Full = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ typical values are at } T_A = +25^{\circ}C, \text{ unless otherwise noted.})^{(1)}$ 

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN <sup>(2)</sup>	<b>TYP</b> <sup>(3)</sup>	MAX <sup>(2)</sup>	UNITS
DC/DC STAGE							
Output Voltage Range	Vout	V <sub>IN</sub> < 0.9*V <sub>OUT</sub>	Full	3.0		5.5	V
Input Voltage Range	VIN		+25°C	2.2		5.5	V
Feedback Voltage	VFB		Full	480	495	510	mV
Switching Frequency	Freq		Full	930	1100	1200	kHz
Switch Current Limit	١L		+25°C	2.15	2.7	3.25	А
Start-Up Current Limit	I <sub>ST</sub>	V <sub>OUT</sub> <v<sub>IN</v<sub>	+25°C		550		mA
Boost Switch On-Resistance	Rds-low	V <sub>OUT</sub> = 5V	+25°C		60		mΩ
Rectifying Switch On-Resistance	$R_{ds\operatorname{-high}}$	V <sub>OUT</sub> = 5V	+25°C		120		mΩ
Line Regulation		V <sub>CC</sub> = 2.2V to V <sub>OUT</sub> - 0.5V	+25°C		0.5		%
Load Regulation			+25°C		0.5		%
Quiescent Current	Ιq	V <sub>EN</sub> = V <sub>CC</sub> = 3.6V, not switching	+25°C		20	30	μA
Shutdown Current	I <sub>SD</sub>	$V_{EN} = 0V, V_{CC} = 3.6V$	+25°C			1	μA
CONTROL STAGE							
EN Input Low Voltage	VIL		Full			0.4	V
EN Input High Voltage	VIH		Full	1.4			V
EN Input Current	I <sub>EN</sub>	Clamped on GND or $V_{CC}$	Full			10	μA
Over-Temperature Protection					150		°C
Over-Temperature Hysteresis					20		°C

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.



### **8.5 TYPICAL CHARACTERISTICS**

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.







Figure 3. Quiescent Current vs Temperature



Figure 5. Output Current vs Efficiency



Figure 2. Output Voltage vs Temperature



Figure 4. Quiescent Current vs Input Voltage



Figure 6. Input Voltage vs Efficiency



# **TYPICAL CHARACTERISTICS**

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



Figure 7. Maximum Output Current vs Input Voltage



Figure 9. Line Transient Response



 $V_{IN}$ =3.6V, RL=2.5K $\Omega$ Figure 11. Output Voltage in Power-Save Mode



Figure 8. Load Transient Response



Figure 10. Start - Up after Enable



Figure 12. Output Voltage in Continuous Mode



### **9 Detailed Description**

#### 9.1 Overview

The RS6651 is a high performance, highly efficient boost converter. To achieve high efficiency the power stage is realized as a synchronous boost topology. For the power switching two actively controlled low  $R_{DS(ON)}$  power MOSFETs are implemented.

### 9.2 Functional Block Diagram



# **10 TYPICAL APPLICATION CIRCUITS**



Figure 13. Typical Single-Cell Li-Ion Input or Dual Dry Cell Input Boost



Figure 14. Supply with an Auxiliary Positive Output



Figure 15. Supply with an Auxiliary Negative Output



### **11** Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### **11.1 APPLICATION INFORMATION**

The RS6651 is a synchronous boost converter operating in 2.2V to 5.5V supply range, for generating a regulated output voltage which can be set to as low as 10% above the supply voltage. An inductor, an output storage capacitor and an input decoupling capacitor should be selected to ensure proper performance desired in a specific application circuit.

### **11.2 Adjustable Output Voltage Version**

An external resistor divider is used to adjust the output voltage. The resistor divider needs to be connected between V<sub>OUT</sub>, FB and GND as shown in Figure 13. When the output voltage is regulated properly, the typical voltage value at the FB pin is 500mV. The maximum recommended value for the output voltage is 5.5 V. The value of the resistor connected between V<sub>OUT</sub> and FB, R1, depending on the needed output voltage (V<sub>OUT</sub>), can be calculated using Equation 1:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R_2 \times \left(\frac{V_{OUT}}{500 \text{mV}} - 1\right)$$
(1)

As an example, if an output voltage of 5.05 V is needed, a 910K $\Omega$  resistor is calculated for R1 when for R2 a 100k $\Omega$  has been selected.

#### **11.3 Inductor Selection**

The device has been optimized to operate with inductance values between  $1\mu$ H and  $4.7\mu$ H. Nevertheless, operation with higher inductance values may be possible. Both average current and peak current should be evaluated in inductor selection. The maximum average inductor current is estimated using Equation 2:

$$L = \frac{V_{OUT \times I_{OUT}}}{V_{IN} \times \eta}$$
(2)

Where, n is the efficiency of the device, which can be set to 0.8 for estimation.

Choosing a proper inductance for a given current ripple value is readily done in design practice. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. Though regulation settle time may rise when load changes. The minimum inductance value for the inductor at given condition is estimated by using Equation 3:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_{L} \times f \times V_{OUT}}$$
(3)

Where f is the switching frequency and  $\Delta IL$  is the ripple current in the inductor, which normally is 20% of the average inductor current or is a design specified value. In typical applications, a 2.2µH inductance is recommended. After choosing an inductor, peak current at maximum loading and lowest input voltage is suggested to be evaluated, which should be lower than the switch current limit of this device as well as the inductor saturation current.

#### **11.4 Selecting the Input Capacitor**

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a at least  $10\mu$ F input capacitor is recommended to improve transient behavior of the regulator and EMI behavior. A ceramic capacitor or a tantalum capacitor with a 100nF ceramic capacitor in parallel, placed close to the IC, is recommended.

#### **11.5 Selecting the Output Capacitors**

The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{\rm MIN} = \frac{I_{\rm OUT} \times (V_{\rm OUT} - V_{\rm IN})}{f \times \Delta V \times V_{\rm OUT}}$$
(4)

Where,



The additional output ripple component caused by ESR is calculated by: Where

$$\Delta V_{\rm ESR} = I_{\rm OUT} \times R_{\rm ESR}$$

(5)

**RS6651** 

Where,

 $\Delta V_{ESR}$  is the output voltage ripple caused by ESR; R<sub>ESR</sub> is the resistor in series with the output capacitor; For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional voltage change may be caused by load transients; the output capacitor has to completely supply the load during the charging phase of the inductor.

The value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of  $10\mu$ F and load transient considerations, the recommended output capacitance value is in the range of  $10\mu$ F to  $47\mu$ F.

Care must be taken when evaluating a ceramic capacitor's derating under the DC bias. Ceramic capacitors can derate by as much as 90% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating should be considered to ensure adequate capacitance at the required output voltage. And instead of using one  $22\mu$ F capacitor, we more recommend two  $10\mu$ F capacitors in parallel.

### **11.6 Layout Guidelines**

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. Careful layout is always important to ensure good performance and stable operation to any kind of switching regulators.

Minimize the high current path including the switch FET, rectifier FET, and the output capacitor;

Minimize the length and area of all traces connected to the SW pin;

Use the GND pin of the device as the center of star-connection to other grounds. Keep the common path to the GND pin, which returns the small signal components and the high current components as short as possible to avoid ground noise.

Place the FB being far away from the SW trace, as the FB node is sensitive and easily picks up noise;

Place the input and the output capacitors as close to the IC as possible;



### 12 PACKAGE OUTLINE DIMENSIONS TSOT23-6<sup>(3)</sup>





**RECOMMENDED LAND PATTERN (Unit: mm)** 





Complex	Dimensions I	n Millimeters	Dimension	s In Inches
Symbol	Min	Max	Min	Мах
A <sup>(1)</sup>		1.100		0.043
A1	0.000	0.100	0.000	0.004
A2	0.700	1.000	0.028	0.039
b	0.300	0.500	0.012	0.020
с	0.080	0.200	0.003	0.008
D <sup>(1)</sup>	2.850	2.950	0.112	0.116
E <sup>(1)</sup>	1.550	1.650	0.061	0.065
E1	2.650	2.950	0.104	0.116
e	0.950(	BSC) <sup>(2)</sup>	0.037(	BSC) <sup>(2)</sup>
e1	1.800	2.000 0		0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.

2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.

3. This drawing is subject to change without notice.



### 13 TAPE AND REEL INFORMATION REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

#### **KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel	Reel Width	A0	B0	K0	P0	P1	P2	W	Pin1
	Diameter	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Quadrant
TSOT23-6	7"	9.5	3.17	3.10	1.10	4.0	4.0	2.0	8.0	Q3

NOTE:

1. All dimensions are nominal.

2. Plastic or metal protrusions of 0.15mm maximum per side are not included.



### **IMPORTANT NOTICE AND DISCLAIMER**

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.