Dual Retriggerable Precision Monostable Multivibrator

1 FEATURES

- **Retriggerable/Resettable Capability**
- **Trigger and Reset Propagation Delays Independent of R_X and C_X**
- **Triggering from rising and falling edge**
- **Power-Supply Range: 2.3V to 6V**
- **Schmitt Trigger Input on A and $\overline{B}$ Inputs**
- **Q and $\overline{Q}$ Buffered Outputs Available**
- **Latch-up performance exceeds 100 mA per JESD 78 Class I Level A**
- **Extended Temperature: -40°C to +125°C**
- **Micro SIZE PACKAGES: SOP16, TSSOP16**

2 APPLICATIONS

- **Blu-ray Players and Home Theaters**
- **Desktop PCs or Notebook PCs**
- **Embedded PCs**
- **GPS: Personal Navigation Devices**
- **Personal Digital Assistant (PDA)**
- **Server PSU**
- **Solid-State Drive (SSD): Client and Enterprise**
- **Video Analytics Servers**
- **Wireless Headsets, Keyboards, and Mice**

3 DESCRIPTIONS

The RS4538 is a dual retriggerable/resettable monostable multivibrator. Each multivibrator has two trigger/retrigger inputs ($\overline{B}$ and A), a direct reset input ($\overline{R}$), two complementary outputs (Q and $\overline{Q}$), and two pins (R_XC_X and C_X) for connecting the external capacitor C_X and resistor R_X to adjust the pulse width of Q and $\overline{Q}$.

The device may be triggered by either the positive or the negative edges of the input pulse. An unused A input should be tied to GND and an unused $\overline{B}$ input should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated.

The duration and accuracy of the output pulse are determined by the external timing components C_X and R_X. The output pulse width (t_W) is equal to $0.66 \times R_X \times C_X$. A LOW level at $\overline{R}$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS4538	SOP16	9.90mm×3.90mm
	TSSOP16	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram

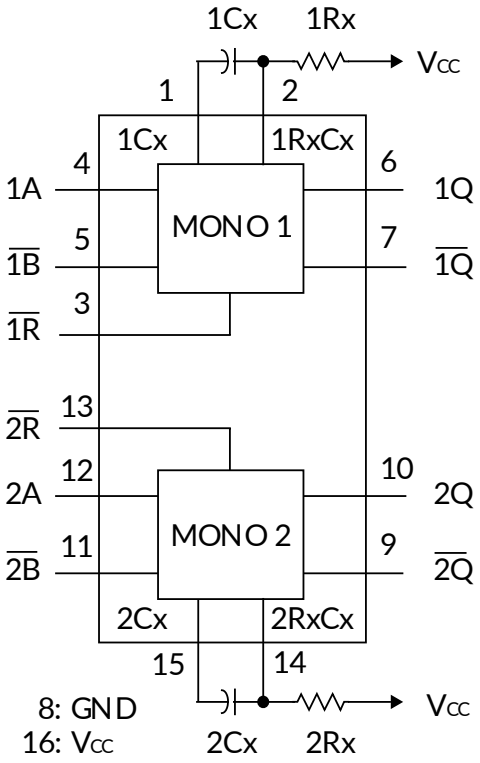

Figure 1. Functional diagram

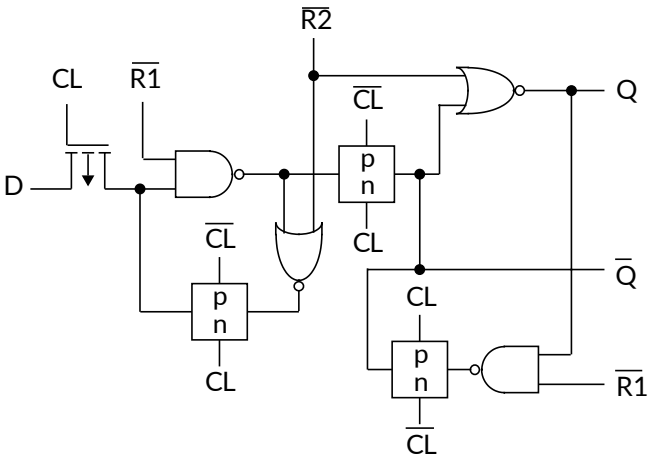

Figure 2. FF detail

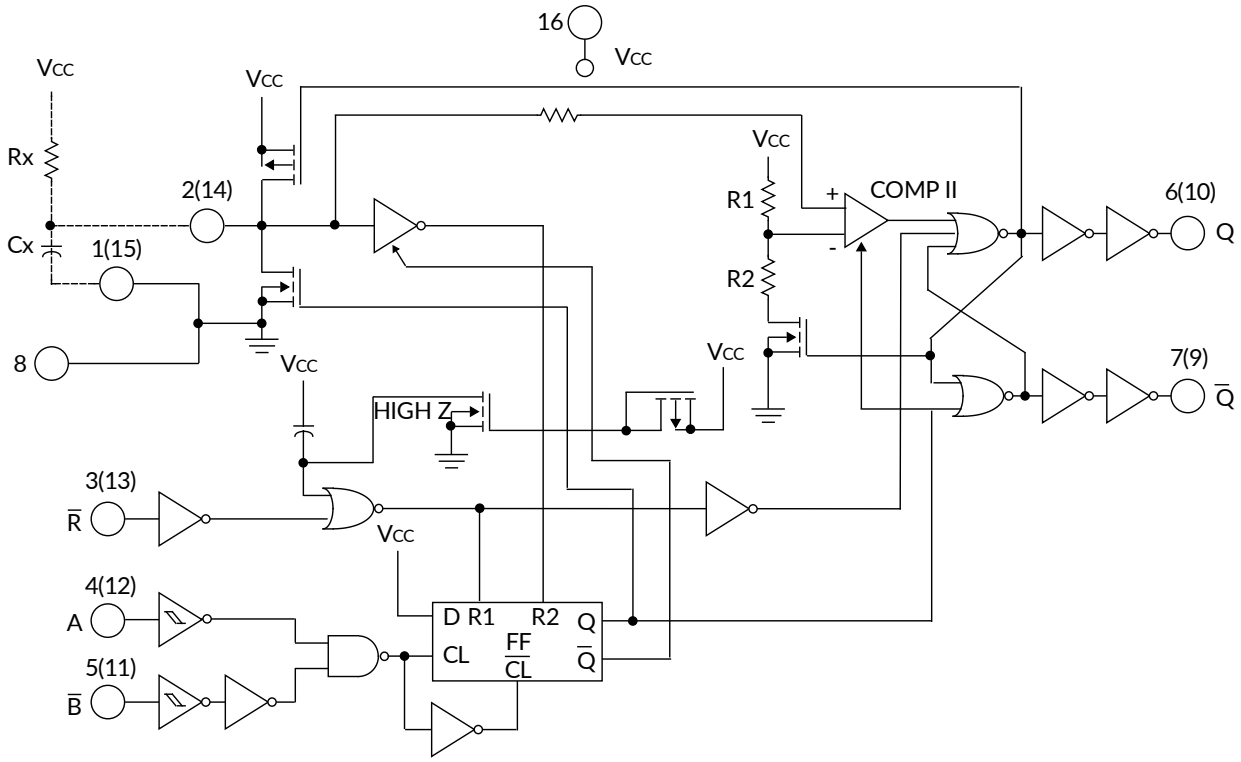

Figure 3. Logic Diagram (1 MONO)

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5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/07/21	Initial version completed
A.2	2023/10/13	1. Update Power-Supply Range: 2.3V to 6V 2. Update ELECTRICAL CHARACTERISTICS
A.2.1	2024/02/29	Modify packaging naming

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS4538	RS4538XTSS16	-40°C ~+125°C	TSSOP16	RS4538	MSL3	Tape and Reel,4000
	RS4538XS16	-40°C ~+125°C	SOP16	RS4538	MSL3	Tape and Reel,4000

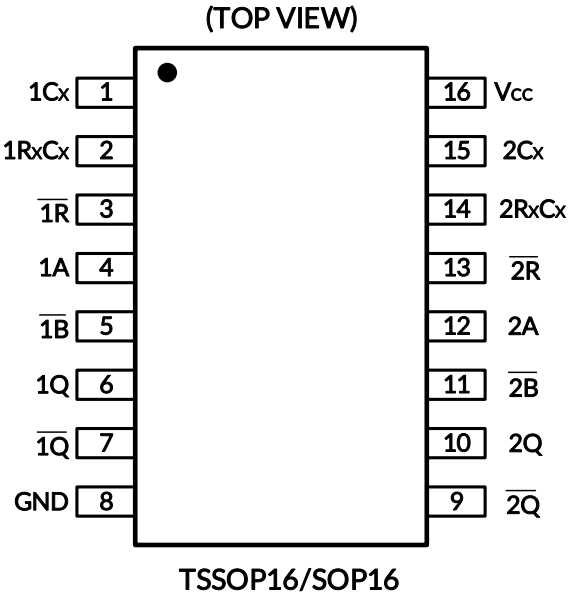
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS



7.1 PIN DESCRIPTION

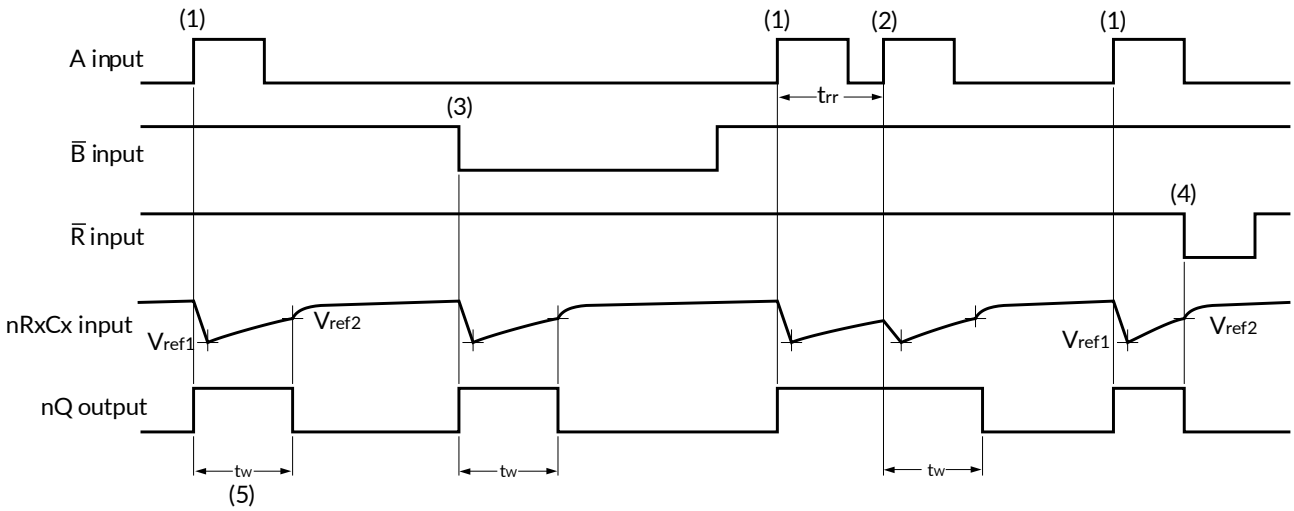
PIN	NAME	I/O (1)	FUNCTION
TSSOP16/SOP16			
1,15	$1C_X$, $2C_X$	-	external capacitor connection (always connected to ground)
2,14	$1R_XC_X$, $2R_XC_X$	-	external capacitor/resistor connection
3,13	$\overline{1R}$, $\overline{2R}$	I	direct reset input (active LOW)
4,12	1A, 2A	I	input (low to high triggered)
5,11	$\overline{1B}$, $\overline{2B}$	I	input (high to low triggered)
6,10	1Q,2Q	O	Output
7,9	$\overline{1Q}$, $\overline{2Q}$	O	Complementary Output (active Low)
8	GND	P	Ground
16	V_{CC}	P	Supply voltage

(1) I=input, O=output, P=power.

7.2 FUNCTIONAL DESCRIPTION

Input			Output	
$\overline{R}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	⎍	⎍
H	L	↓	⎍	⎍
X	H	X	L	H
X	X	L	L	H

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant;
↑ = Transition from Low to High, ↓ = Transition from High to Low;
⎍ One High Level Pulse, ⎍ One Low Level Pulse.



(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) $t_W = 0.66 \times R_X \times C_X$ (see also Figure 5).

Figure 4. Timing diagram and retrigger times

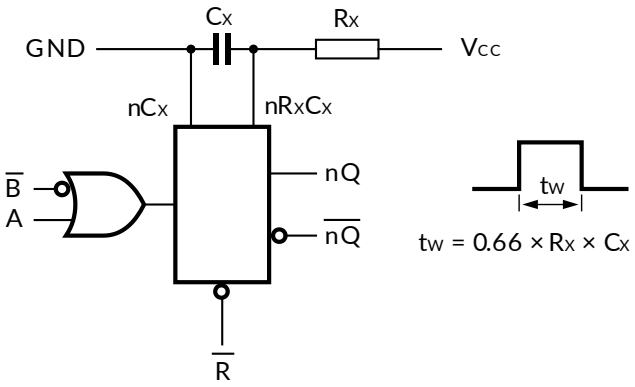


Figure 5. Connection of the external timing components R_X and C_X

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	DC Supply Voltage		-0.5	7	V
I_{IK}	DC Input Diode Current	For V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	DC Output Diode Current	For V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	DC Output Source or Sink Current per Output Pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
I_{CC}	DC V_{CC} or Ground Current			±50	mA
θ_{JA}	Package thermal impedance (2)	TSSOP16		45	°C/W
		SOP16		150	
T_J	Junction temperature (3)		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), JEDEC EIA/ JESD22 - A114	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	V
		Machine model (MM), JESD22-A115C (2010)	±100	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.)

9.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC} (1)		2.3	6	V
DC Input voltage	V_I		0	V_{CC}	V
DC Output voltage	V_O		0	V_{CC}	V
Input Rise and Fall Times	t_r, t_f	V_{CC}=2.5V		800	ns
		V_{CC}=4.5V		500	
		V_{CC}=6V		400	
Operating temperature	T_A		-40	+125	°C

(1) Unless otherwise specified, all voltages are referenced to ground.

9.2 DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	Operating free-air temperature (T_A)						UNIT
					25°C			-40°C to 85°C		-40°C to 125°C	
		V_I (V)	I_O (mA)		MIN(1)	TYP(2)	MAX(1)	MIN	MAX	MIN	MAX
High Level Input Voltage	V_{IH}			2.5	1.85			1.85		1.85	V
				4.5	3.15			3.15		3.15	V
				6	4.2			4.2		4.2	V
Low Level Input Voltage	V_{IL}			2.5			0.65		0.65		0.65	V
				4.5			1.35		1.35		1.35	V
				6			1.8		1.8		1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2.5	2.4			2.4		2.4		V
			-0.02	4.5	4.4			4.4		4.4		V
			-0.02	6	5.9			5.9		5.9		V
			-4	4.5	3.98			3.84		3.7		V
			-8	6	5.48			5.34		5.2		V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2.5			0.1		0.1		0.1	V
			0.02	4.5			0.1		0.1		0.1	V
			0.02	6			0.1		0.1		0.1	V
			4	4.5			0.26		0.33		0.4	V
			8	6			0.26		0.33		0.4	V
Input Leakage Current A, $\overline{B}$, $\overline{R}$	I_I	V_{CC} or GND		6			±1		±2		±2	μA
Input Leakage Current R_XC_X (3)				6			±0.05		±0.5		±0.5	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6			8		80		160	μA
Active Device Current Q = High & Pins 2, 14 at $V_{CC}/4$	I_{CC}	V_{CC} or GND	0	6			0.6		0.8		1	mA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(3) When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.

9.3 Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC}(V)	Operating free-air temperature (T_A)							UNIT
			25°C			-40°C to 85°C		-40°C to 125°C		
			MIN(1)	TYP(2)	MAX(1)	MIN	MAX	MIN	MAX	
Input Pulse Widths A, $\overline{B}$	t_{WH}, t_{WL}	2.5	65			80		100		ns
		4.5	16			20		24		ns
		6	14			17		20		ns
$\overline{R}$	t_{WL}	2.5	65			80		100		ns
		4.5	16			20		24		ns
		6	14			17		20		ns
Reset Recovery Time	t_{REC}	2.5	35	6		45		55		ns
		4.5	7	2		9		11		ns
		6	6	2		8		9		ns
Retrigger Time	t_{rr}	5		175						ns
External Timing Resistor	R_X	2.3	5							kΩ
		5	2							

(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

9.4 Switching Specifications

C_L = 50pF, Input t_r, t_f = 10ns, R_X = 10KΩ, C_X = 0.

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC}(V)	Operating free-air temperature (T_A)							UNIT
				25°C			-40°C to 85°C		-40°C to 125°C		
				MIN(1)	TYP(2)	MAX(1)	MIN	MAX	MIN	MAX	
Propagation Delay A, $\overline{B}$ to Q	t_{PLH}	C_L = 50pF	2.5		22	32		37		39	ns
			4.5		17	24		25		26	ns
		C_L = 15pF	5		16	23		24		25	ns
		C_L = 50pF	6		15	22		23		24	ns
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2.5		21	31		33		34	ns
			4.5		16	22		24		25	ns
		C_L = 15pF	5		15	21		23		24	ns
		C_L = 50pF	6		14	20		22		23	ns
$\overline{R}$ to Q	t_{PHL}	C_L = 50pF	2.5		19	28		29		31	ns
			4.5		13	20		21		22	ns
		C_L = 15pF	5		12	18		19		21	ns
		C_L = 50pF	6		11	17		18		19	ns
$\overline{R}$ to $\overline{Q}$	t_{PLH}	C_L = 50pF	2.5		17	25		26		28	ns
			4.5		12	17		18		19	ns
		C_L = 15pF	5		11	16		17		18	ns
		C_L = 50pF	6		10	15		16		17	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2.5		10	15		16		17	ns
			4.5		8	11		13		14	ns
			6		7	10		11		13	ns
Output Pulse Width R_X = 10kΩ, C_X= 0.1 μF	t_W	C_L = 50pF	3	0.63	0.68	0.75	0.58	0.78	0.58	0.78	ms
			5	0.59	0.66	0.73	0.56	0.76	0.56	0.76	ms
Power Dissipation Capacitance (3)(4)	C_{pd}	C_L = 15pF	5		162						pF
Input Capacitance	C_{in}	C_L = 50pF			10						pF

NOTES:

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(3) C_{PD} is used to determine the dynamic power consumption, per one shot.

(4) $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \sum(C_L V_{CC}^2 f_O)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, C_X = external capacitance, V_{CC} = supply voltage assuming $f_i \ll 1/ t_W$.

9.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

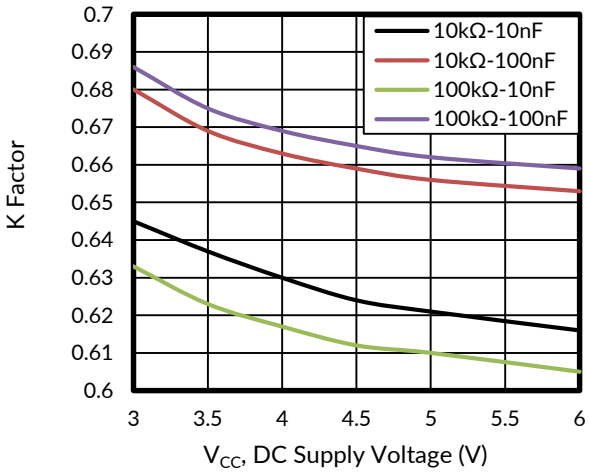


Figure 6. K Factor vs DC Supply Voltage (V_{CC})

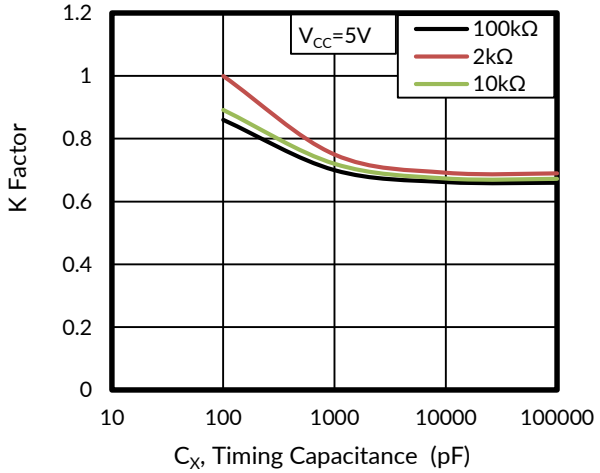


Figure 7. K Factor vs C_X, Timing Capacitance

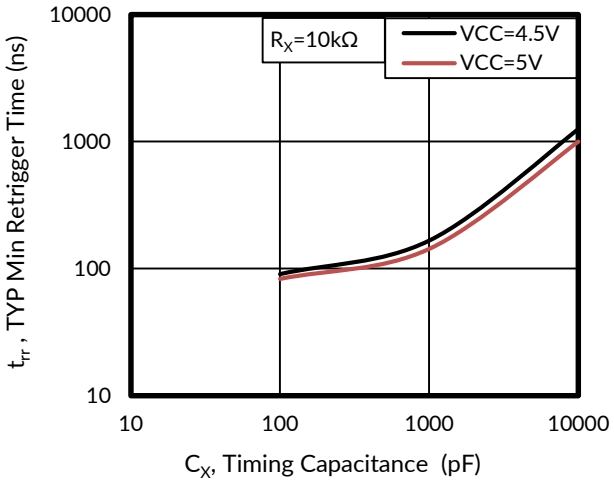
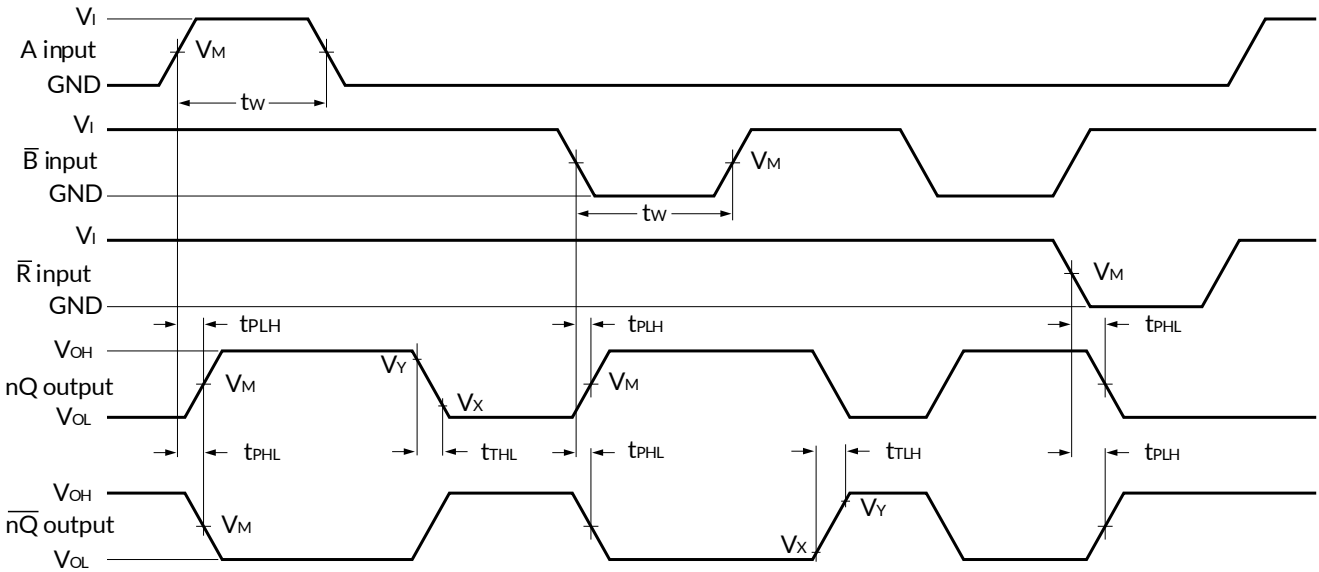


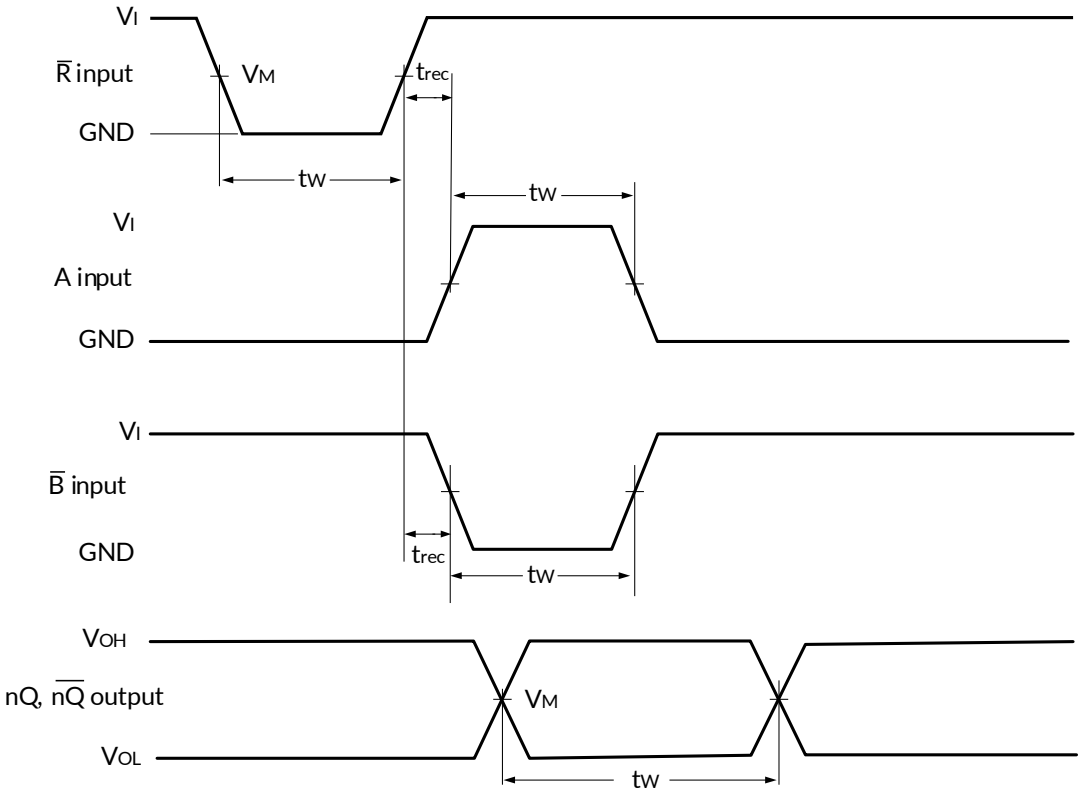
Figure 8. Minimum Retrigger Time vs Timing Capacitance

10 Test Circuits and Waveforms



Measurement points are given in Table 1.
Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 9. Waveforms showing propagation delays and transition times

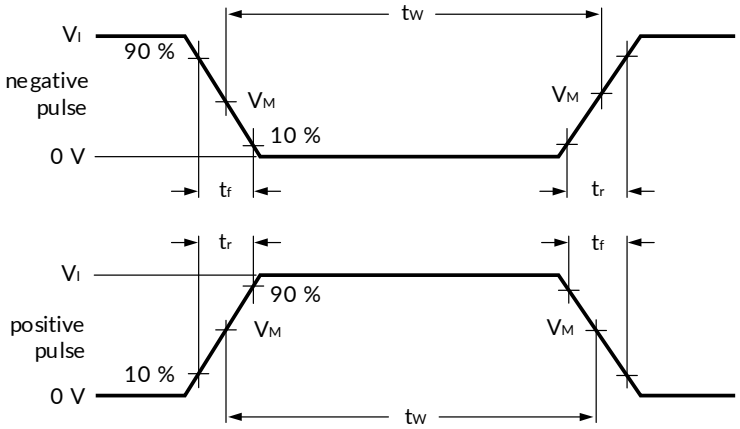


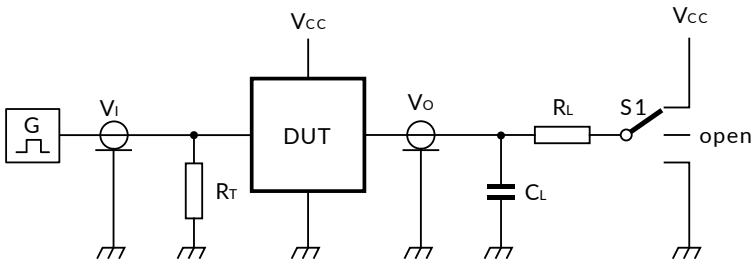
Measurement points are given in Table 1.
Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 10. Waveforms showing A, $\overline{B}$, nQ, $\overline{nQ}$ pulse widths and recovery time

Table 1. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
0.5V_{CC}	0.5V_{CC}	0.1V_{CC}	0.9V_{CC}





Test data is given in Table 2.
Definitions test circuit:
R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator.
C_L = Load capacitance including jig and probe capacitance.
R_L = Load resistance.
S1 = Test selection switch

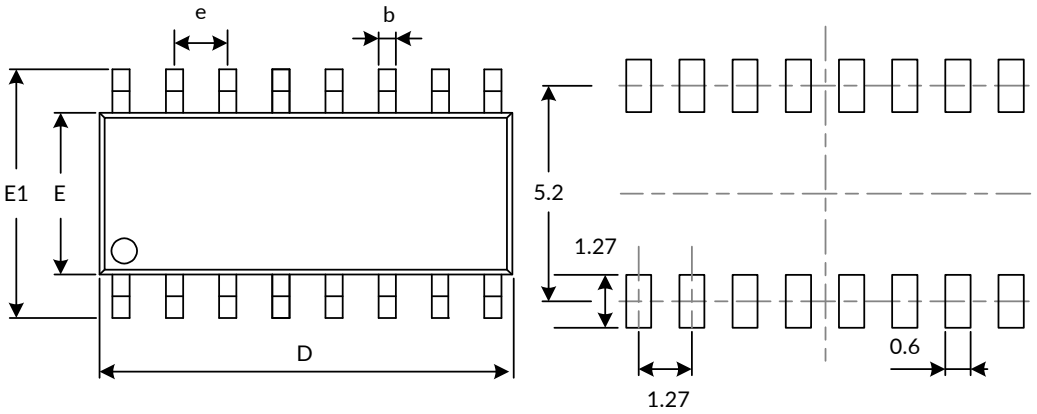
Figure 11. Test circuit for measuring switching times

Table 2. Test data

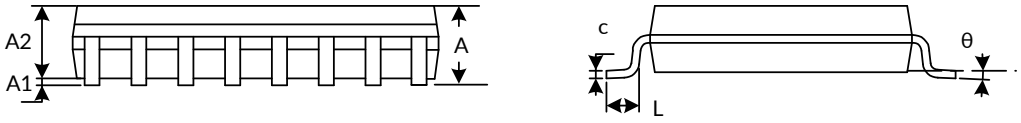
Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	10ns	15pF, 50pF	1kΩ	open

11 PACKAGE OUTLINE DIMENSIONS

SOP16 (3)



RECOMMENDED LAND PATTERN (Unit: mm)

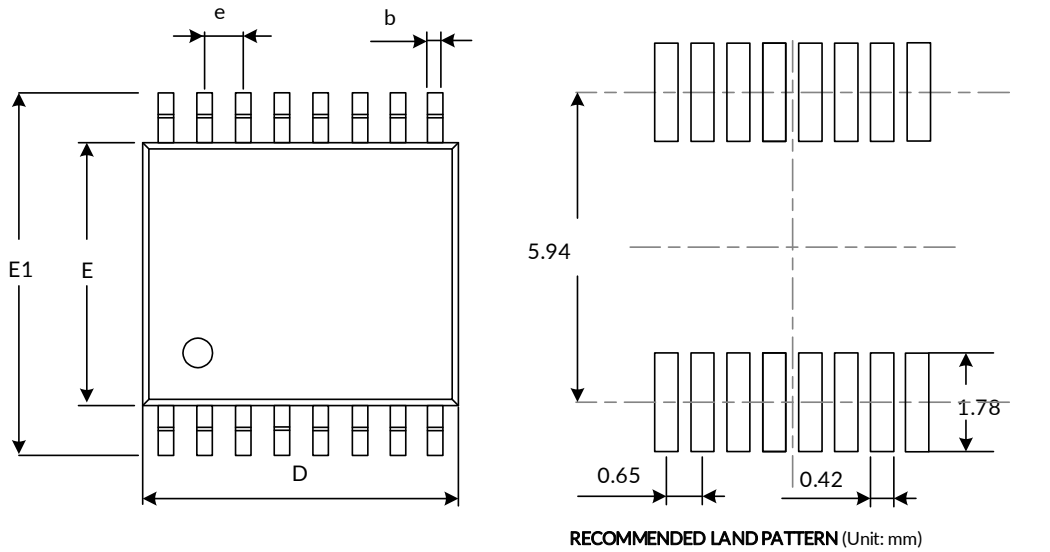


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D (1)	9.800	10.200	0.386	0.402
E (1)	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27(BSC) (2)		0.050(BSC) (2)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP16 (3)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.02	0.028
H	0.25TYP		0.01TYP	
θ	1°	7°	1°	7°

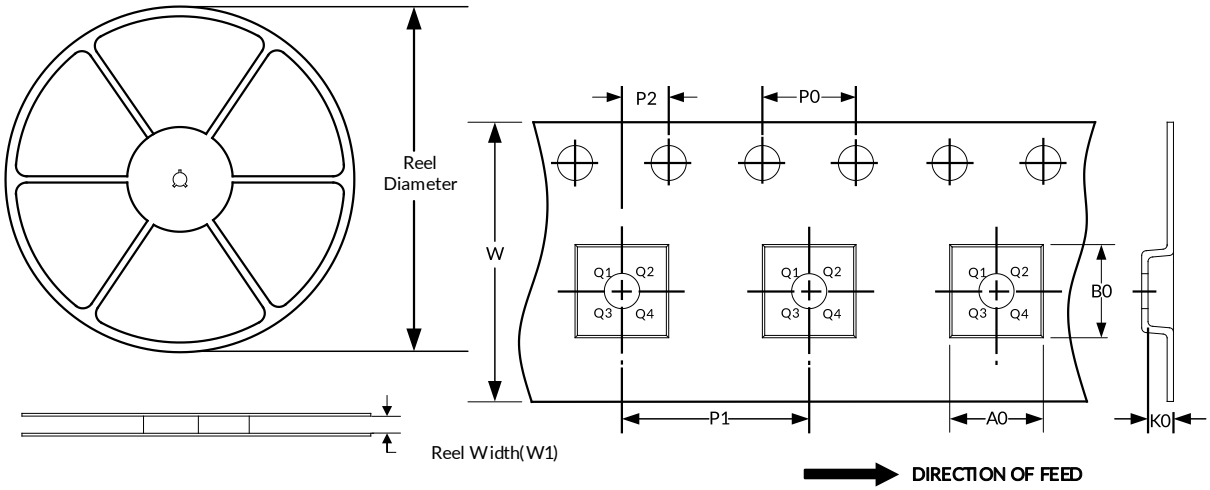
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP16	13”	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP16	13”	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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