RS29539 Low-Voltage 16-Bit I²C and SMBus Low-Power I/O Expander with Interrupt Output, Reset Pin, and Configuration Registers

1 FEATURES

- **I²C to Parallel Port Expander**
- **Wide Power Supply Voltage Range of 1.65V to 5.5V**
- **Low Standby-Current Consumption**
- **Open-Drain Active-Low Interrupt Output**
- **Active-Low Reset Input**
- **5V Tolerant I/O Ports**
- **Compatible With Most Microcontrollers**
- **400kHz Fast I²C Bus**
- **Input and Output Configuration Register**
- **Polarity Inversion Register**
- **Internal Power-on Reset**
- **No Glitch on Power Up**
- **Noise Filter on SCL and SDA Inputs**
- **Address by Two Hardware Address Pins for Use of up to Four Devices**
- **Latched Outputs with High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000V Human-Body Model (A114-A)**
  - **1000V Charged-Device Model (C101)**

2 APPLICATIONS

- **Servers**
- **Routers (Telecom Switching Equipment)**
- **Personal Computers, smartphones**
- **Industrial Automation**
- **I²C GPIO Expansion**

3 DESCRIPTIONS

The RS29539 is a 24-pin device that provides 16 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus protocol). The device can operate with a power supply voltage (V_{CC}) range from 1.65 V to 5.5 V. The device supports 100kHz (I²C Standard mode) and 400kHz (I²C Fast mode) clock frequencies. I/O expanders such as the RS29539 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

The features of the RS29539 include an interrupt that is generated on the $\overline{\text{INT}}$ pin whenever an input port changes state. The A0 and A1 hardware selectable address pins allow up to four RS29539 devices on the same I²C bus. The device can be reset to its default state by cycling the power supply and causing a power-on-reset. Also, the RS29539 has a hardware $\overline{\text{RESET}}$ pin that can be used to reset the device to its default state.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS29539	TSSOP24	7.80mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2024/08/08	Preliminary version completed
A.1	2025/02/27	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS29539	RS29539XTSS24	-40°C ~125°C	TSSOP24	RS29539	MSL3	Tape and Reel, 4000

NOTE:

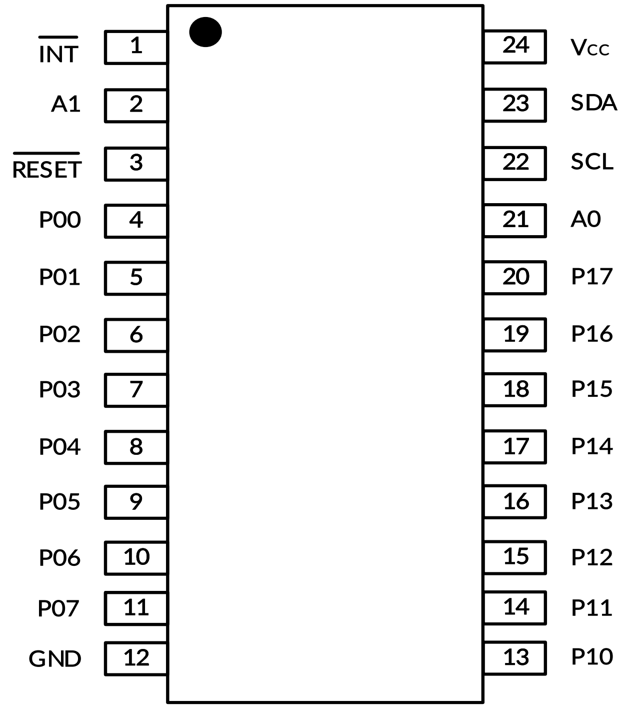
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATIONS AND FUNCTIONS

(TOP VIEW)



TSSOP24

PIN DESCRIPTION

PIN	NAME	TYPE (2)	DESCRIPTION
TSSOP24			
21	A0	I	Address input 0. Connect directly to V_{CC} or ground
2	A1	I	Address input 1. Connect directly to V_{CC} or ground
3	$\overline{RESET}$	I	Active-low reset input. Connect to V_{CC} through a pull-up resistor if no active connection is used
12	GND	—	Ground
1	$\overline{INT}$	O	Interrupt output. Connect to V_{CC} through an external pull-up resistor
4	P00 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
5	P01 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
6	P02 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
7	P03 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
8	P04 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
9	P05 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
10	P06 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
11	P07 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input

13	P10 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
14	P11 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
15	P12 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
16	P13 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
17	P14 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
18	P15 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
19	P16 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
20	P17 (1)	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
22	SCL	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
23	SDA	I	Serial data bus. Connect to V_{CC} through a pull-up resistor
24	V_{CC}	—	Supply voltage

(1) If port is unused, it must be tied to either V_{CC} or GND through a resistor of moderate value (about 10kΩ).
(2) I=input, O=output, I/O=input and output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage		-0.5	6.5	V
V_I	Input voltage (2)		-0.5	6.5	V
V_O	Output voltage (2)		-0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		-20	mA
I_{OK}	Output clamp current	$V_O < 0$		-20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		-50	mA
I_{CC}	Continuous current through GND			-250	mA
	Continuous current through V_{CC}			160	mA
θ_{JA}	Package thermal impedance (3)	TSSOP24		35	°C/W
T_J	Junction Temperature (4)			100	°C
T_{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM)	±2000	V
		Charged-Device Model (CDM)	±1000	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

PARAMETER		CONDITIONS		MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA		0.7 × V_{CC}	V_{CC} (1)	V
		A2–A0, P07–P00, P17–P10		0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA, A2–A0, P07–P00, P17–P10		–0.5	0.3 × V_{CC}	V
I_{OH}	High-level output current	P07–P00, P17–P10			-10	mA
I_{OL}	Low-level output current (2)	P07–P00, P17–P10	T_J ≤ 65°C		25	mA
			T_J ≤ 85°C		18	
			T_J ≤ 100°C		11	
I_{OL}	Low-level output current (2)	$\overline{INT}$, SDA	T_J ≤ 85°C		6	mA
			T_J ≤ 100°C		3.5	
T_A	Operating free-air temperature			–40	125	°C

(1) For voltages applied above V_{CC}, an increase in I_{CC} results.

(2) The values shown apply to specific junction temperatures, which depend on the $R_{\theta JA}$ of the package used. See the Calculating Junction Temperature and Power Dissipation section on how to calculate the junction temperature.

7.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = −18 mA	1.65 V to 5.5 V	-1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		$V_I = V_{CC}$ or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		$V_I = V_{CC}$ or GND, I_O = 0		0.8			V
V_{OH}	P-port high-level output voltage (2)		I_{OH} = −8 mA	1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				4.75 V	4.1			
			I_{OH} = −10 mA	1.65 V	1			
				2.3 V	1.7			
				3 V	2.5			
				4.75 V	4			
I_{OL}	Low-level output current	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
		P port (3)	V_{OL} = 0.5 V	1.65 V to 5.5 V	8			
			V_{OL} = 0.7 V	1.65 V to 5.5 V	10			
		$\overline{INT}$	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			
I_I	Input leakage current	SCL, SDA Input leakage	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V			±1	µA
		A2–A0 Input leakage	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V			±1	
I_{IH}	Input high leakage current	P port	$V_I = V_{CC}$	1.65 V to 5.5 V			1	µA
I_{IL}	Input low leakage current	P port	V_I = GND	1.65 V to 5.5 V			−1	µA
I_{CC}	Quiescent current	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz, No load	5.5 V			75	µA
				3.6 V			39	
				2.7 V			26	
				1.95 V			17	
				1.65 V			15	
		Standby mode	$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.5	3.9	
				3.6 V		0.9	2.2	
				2.7 V		0.6	1.8	
				1.95 V		0.6	1.5	
			V_I = GND, I_O = 0, I/O =inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.5	8.7	
				3.6 V		0.9	4	
				2.7 V		0.6	3	
				1.95 V		0.4	2.2	
C_I	Input capacitance	SCL	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		3	8	pF
C_{io}	Input-output pin capacitance	SDA	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		3	9.5	pF
		P port	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		3.7	9.5	

(1) All typical values are at nominal supply voltage (1.8V, 2.5V, 3.3V, or 5V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

7.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I²C BUS—STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
I²C BUS—FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC}/5.5V)	300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus	20 × (V_{CC}/5.5V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF

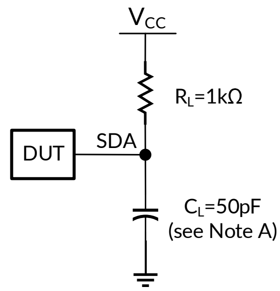
7.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (1)

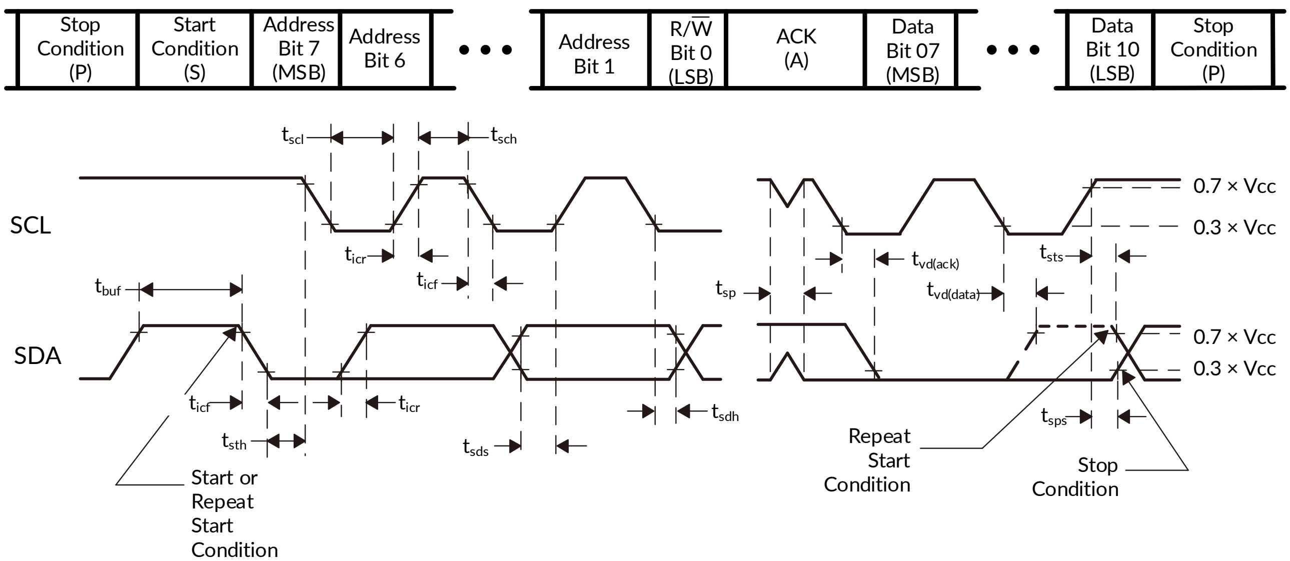
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid; For V_{CC} = 2.3 V–5.5 V	SCL	P port		200	ns
	Output data valid; For V_{CC} = 1.65 V–2.3 V				300	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8 PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION

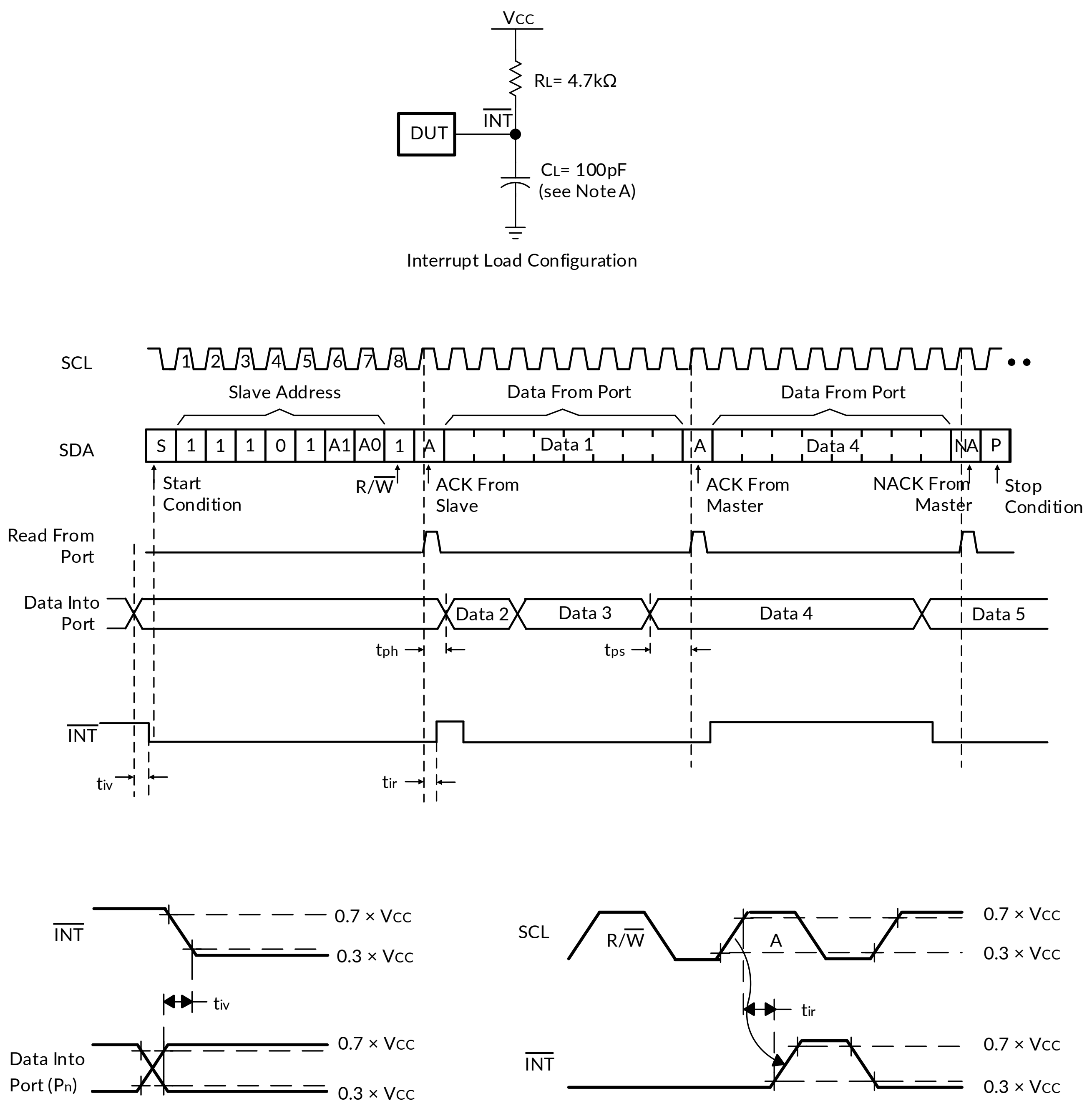


VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

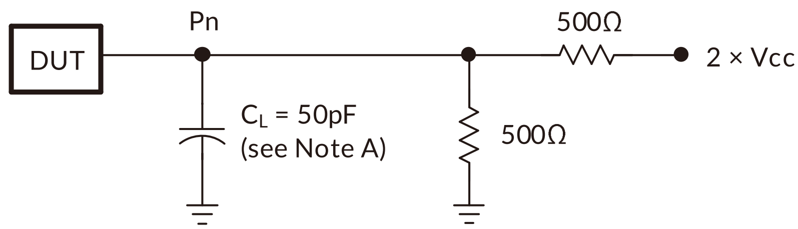
A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

Figure 1. I^2C Interface Load Circuit and Voltage Waveforms

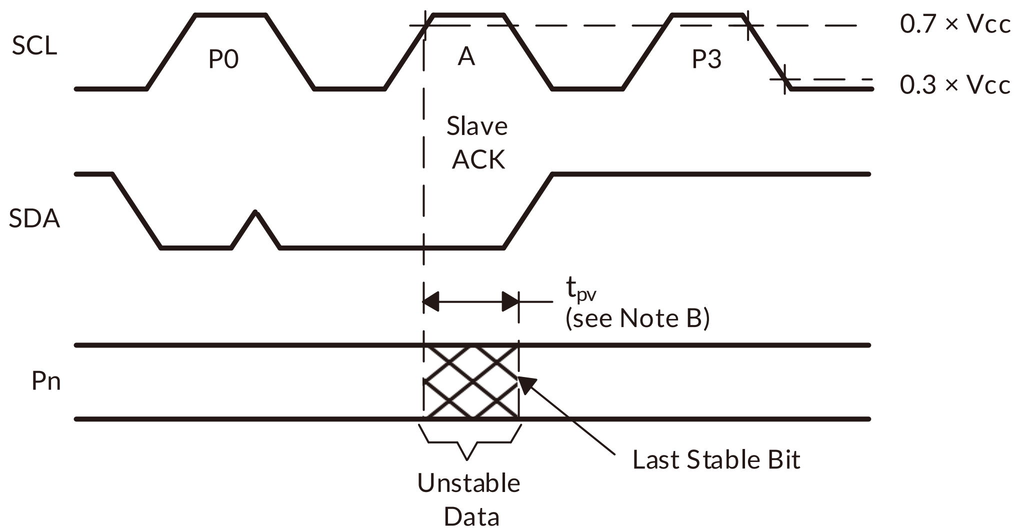


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r / t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

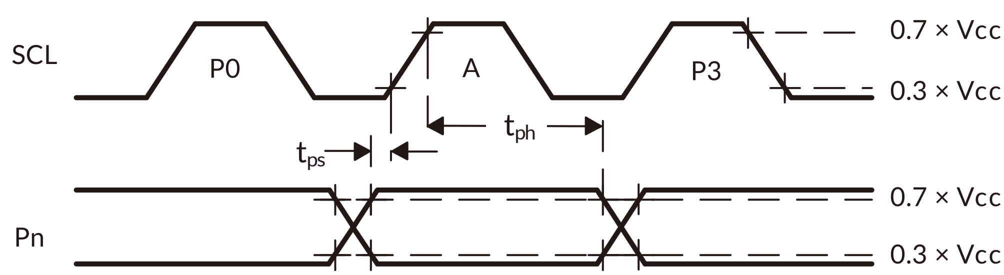
Figure 2. Interrupt Load Circuit and Voltage Waveforms



P-Port Load Configuration



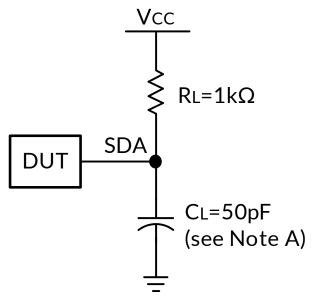
Write Mode (R/$\overline{W}$ =0)



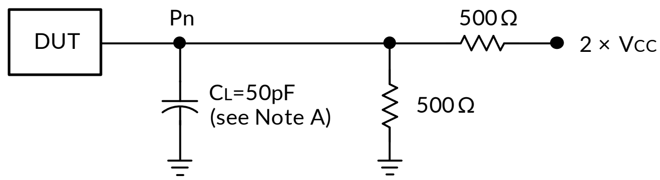
Read Mode (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r /t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

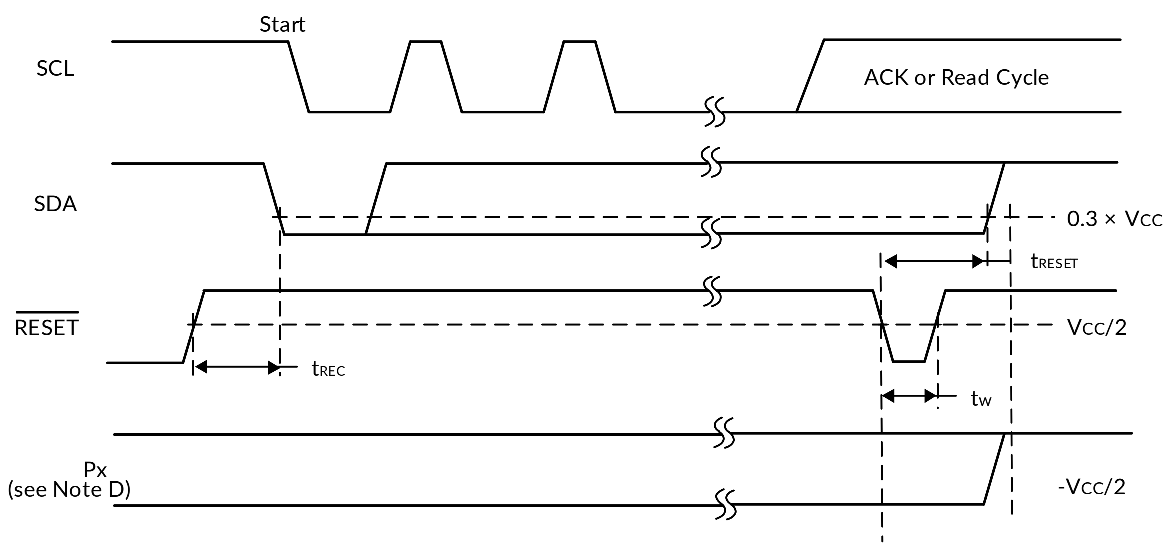
Figure 3. P-Port Load Circuit and Voltage Waveforms



SDA Load Configuration



P-Port Load Configuration



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r /t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

Figure 4. Reset Load Circuits and Voltage Waveforms

9 DETAILED DESCRIPTION

9.1 Overview

The RS29539 device is a 16-bit I/O expander for the I²C bus and is designed for 1.65V to 5.5V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface, serial clock (SCL) and serial data (SDA).

The RS29539 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the RS29539 in the event of a time-out or other improper operation by asserting a low in the $\overline{RESET}$ input. The power-on reset puts the registers in their default state and initializes the I²C-SMBus state machine. Asserting $\overline{RESET}$ causes the same reset-initialization to occur without depowering the part.

The RS29539 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

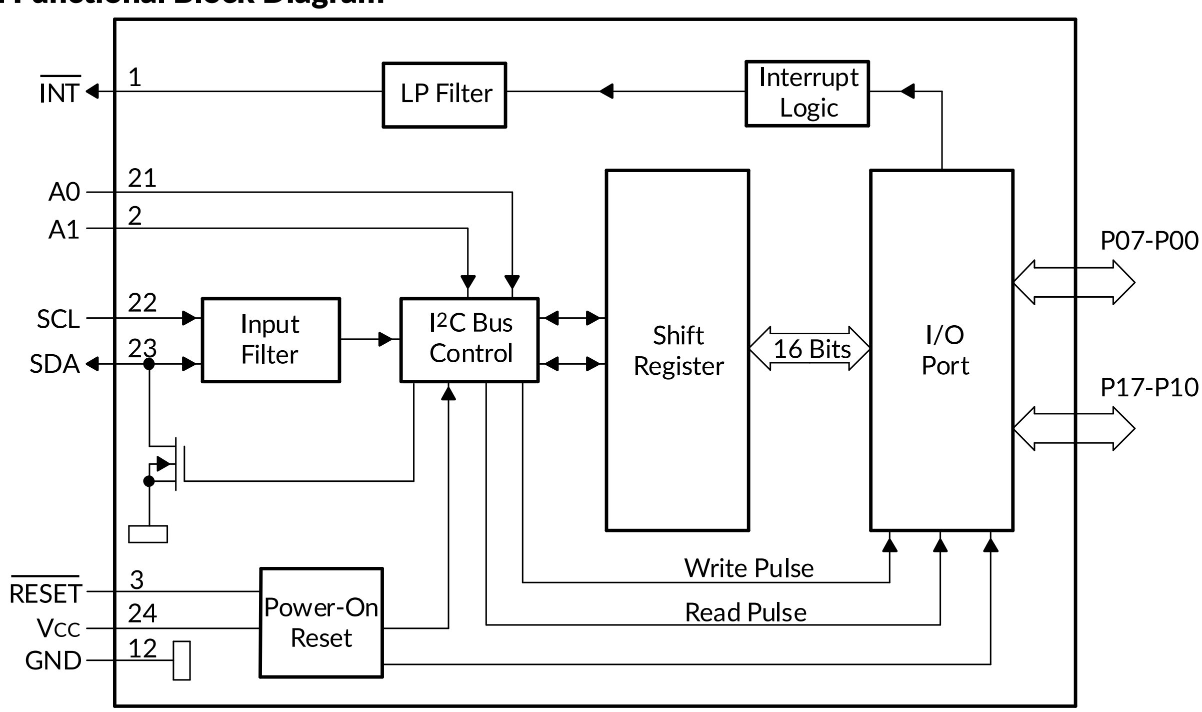
$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Thus, the RS29539 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The RS29539 device is similar to the RS29555, except for the removal of the internal I/O pull-up resistor, which greatly reduces power consumption when the I/Os are held low, replacement of A2 with $\overline{RESET}$, and a different address range.

Two hardware pins (A0 and A1) are used to program and vary the fixed I²C address and allow up to four devices to share the same I²C bus or SMBus.

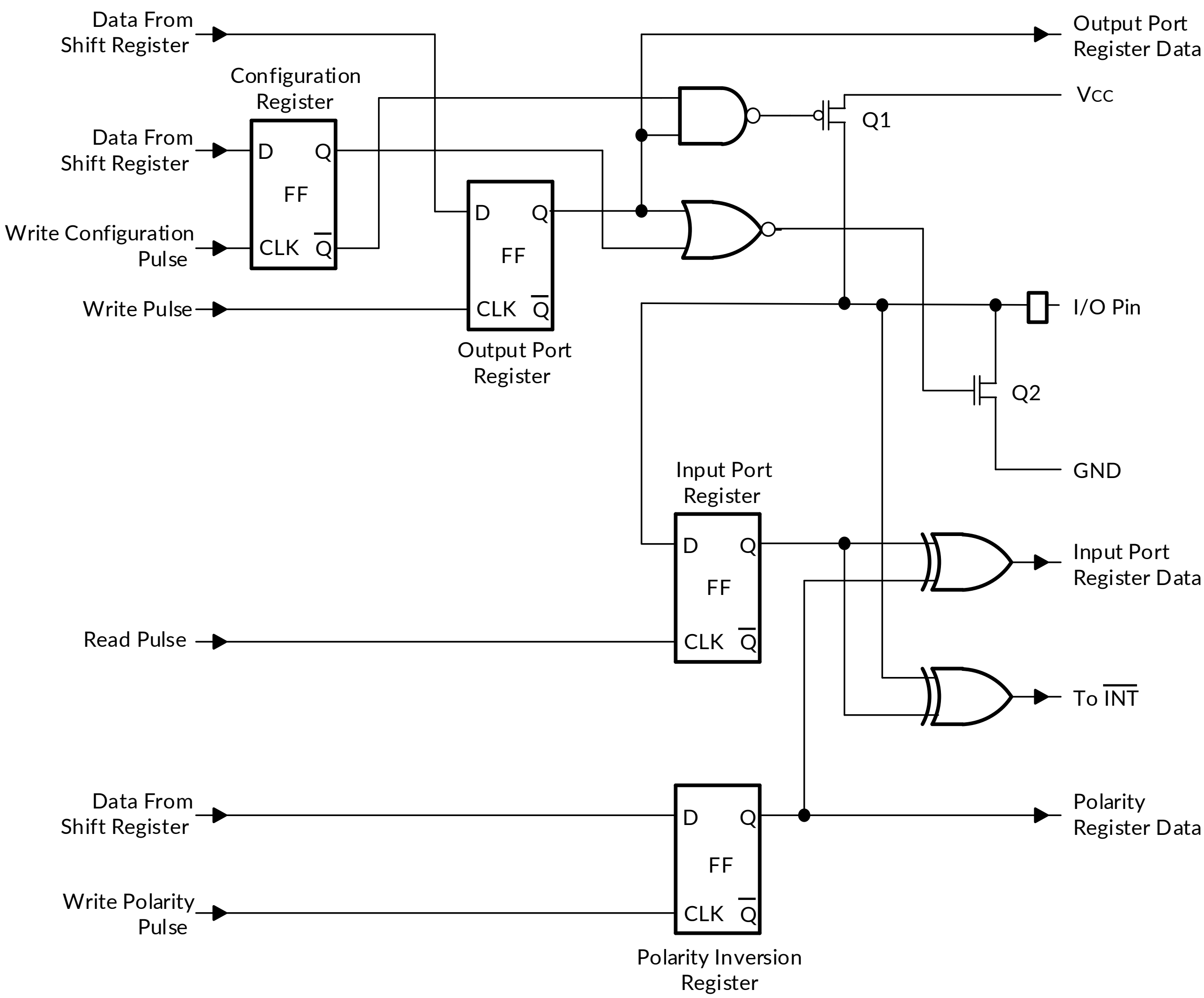
9.2 Functional Block Diagram



A. Pin numbers shown are for the TSSOP24 package.

B. All I/Os are set to inputs at reset.

Figure 5. Logic Diagram (Positive Logic)



At power-on reset, all registers return to default values.

Figure 6. Simplified Schematic of P-Port I/Os

9.3 Feature Description

9.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.
If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

9.3.2 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The RS29539 registers and I^2C/SMBus state machine are held in their default states until $\overline{\text{RESET}}$ is once again high. This input requires a pull-up resistor to V_{CC}, if no active connection is used.

9.3.3 Interrupt ($\overline{\text{INT}}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{\text{INT}}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.
Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.
$\overline{\text{INT}}$ has an open-drain structure and requires a pull-up resistor to V_{CC}.

9.4 Device Functional Modes

9.4.1 Power-On Reset (POR)

When power (from 0V) is applied to V_{CC}, an internal power-on reset circuit holds the RS29539 in a reset condition until V_{CC} has reached V_{PORR}. At that time, the reset condition is released, and the RS29539 registers and I^2C-SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

9.5 Programming

9.5.1 I^2C Interface

The RS29539 has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.
The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See Table 1.
Figure 7 and Figure 8 show the general procedure for a master to access a slave device:
1. If a master wants to send data to a slave:

- Master-transmitter sends a START condition and addresses the slave-receiver.
- Master-transmitter sends data to slave-receiver.
- Master-transmitter terminates the transfer with a STOP condition.

2. If a master wants to receive or read data from a slave:
- Master-receiver sends a START condition and addresses the slave-transmitter.
- Master-receiver sends the requested register to read to slave-transmitter.
- Master-receiver receives data from the slave-transmitter.
- Master-receiver terminates the transfer with a STOP condition.

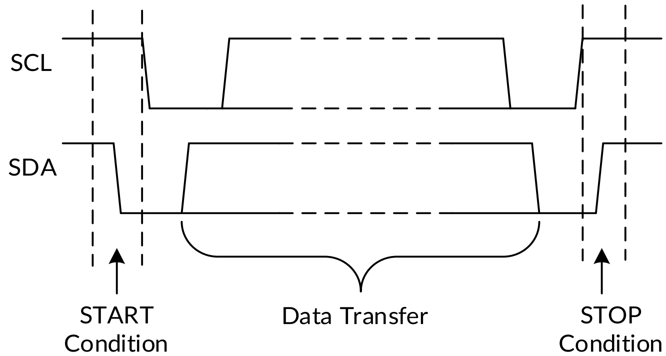


Figure 7. Definition of Start and Stop Conditions

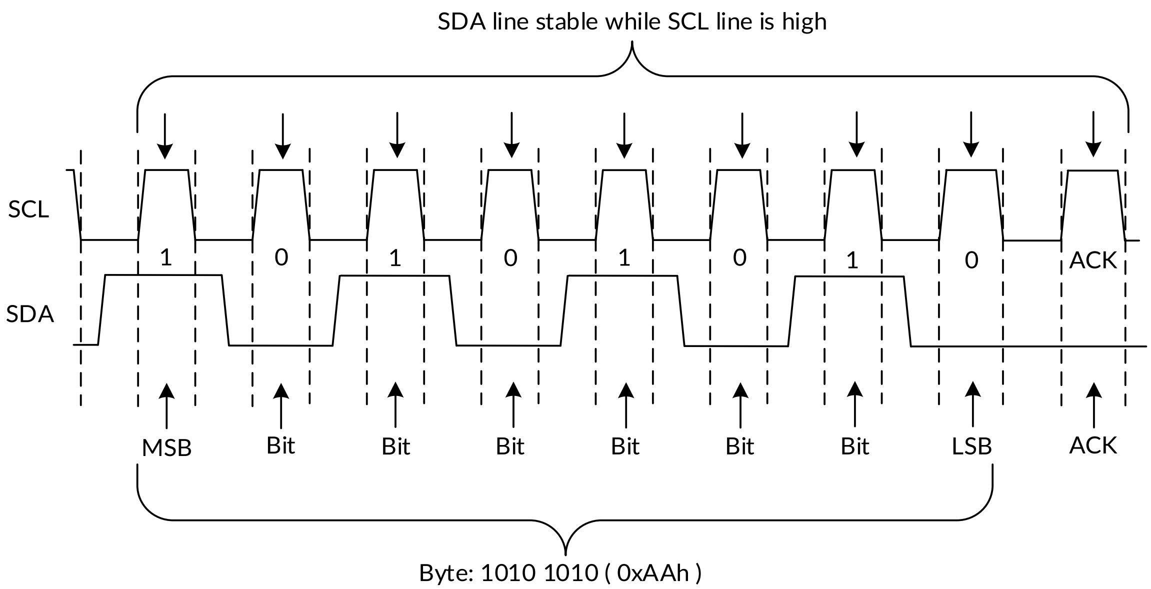


Figure 8. Bit Transfer

Table 1 shows the interface definition.

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	H	H	H	L	H	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

9.5.1.1 Bus Transactions

Data is exchanged between the master and the RS29539 through write and read commands, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

9.5.1.1.1 Writes

To write on the I^2C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See the Register Descriptions section to see list of the RS29539's internal registers and a description of each one.

Figure 9 shows an example of writing a single byte to a slave register.

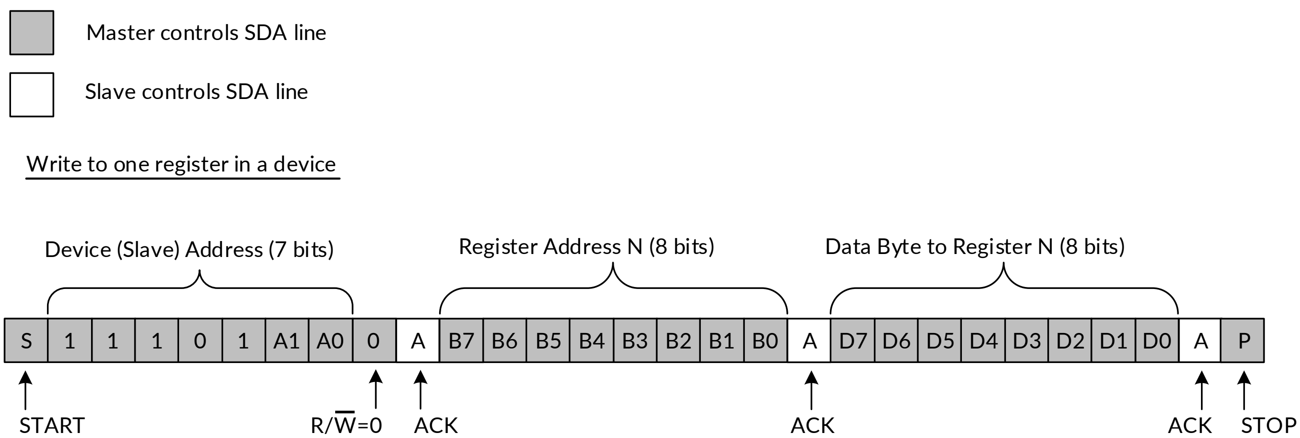


Figure 9. Write to Register

Figure 10 shows the Write to the Polarity Inversion Register.

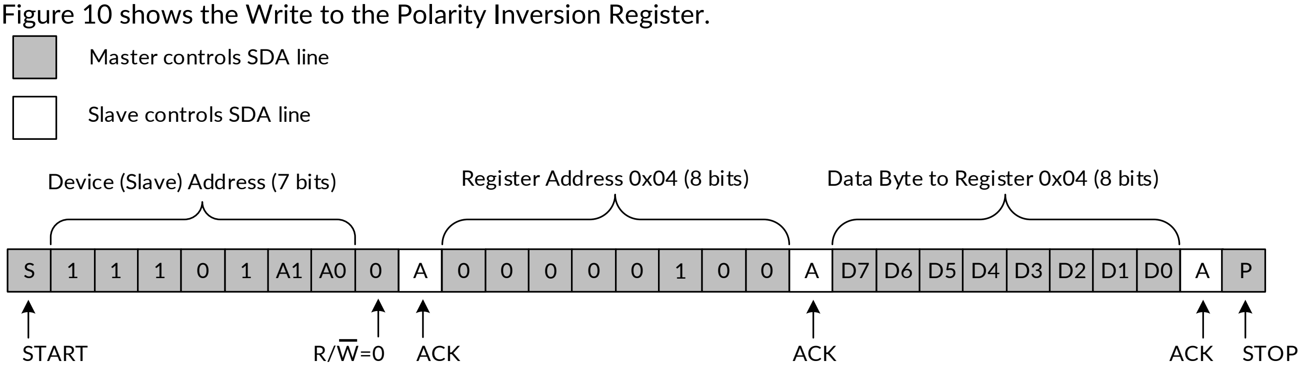


Figure 10. Write to the Polarity Inversion Register

Figure 11 shows the Write to Output Port Registers.

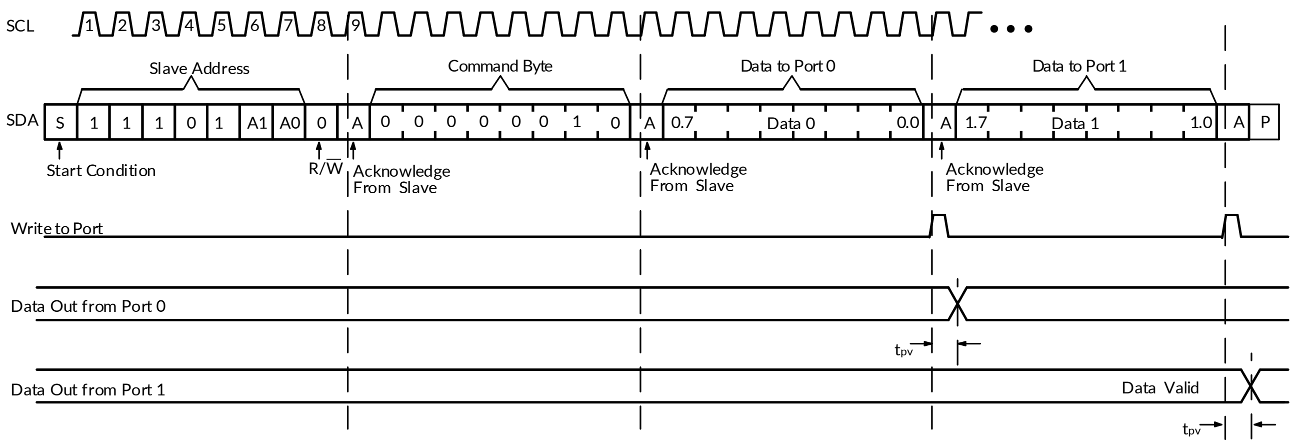


Figure 11. Write to Output Port Registers

9.5.1.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

See the Control Register and Command Byte section to see list of the RS29539's internal registers and a description of each one.

Figure 12 shows an example of reading a single byte from a slave register.

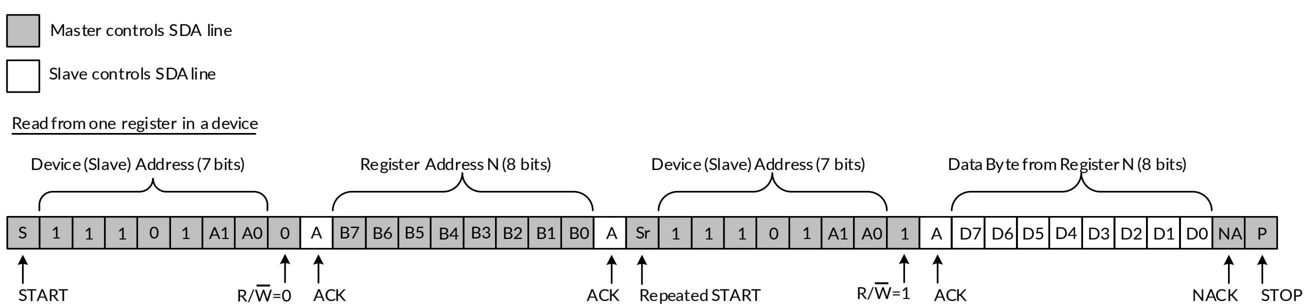
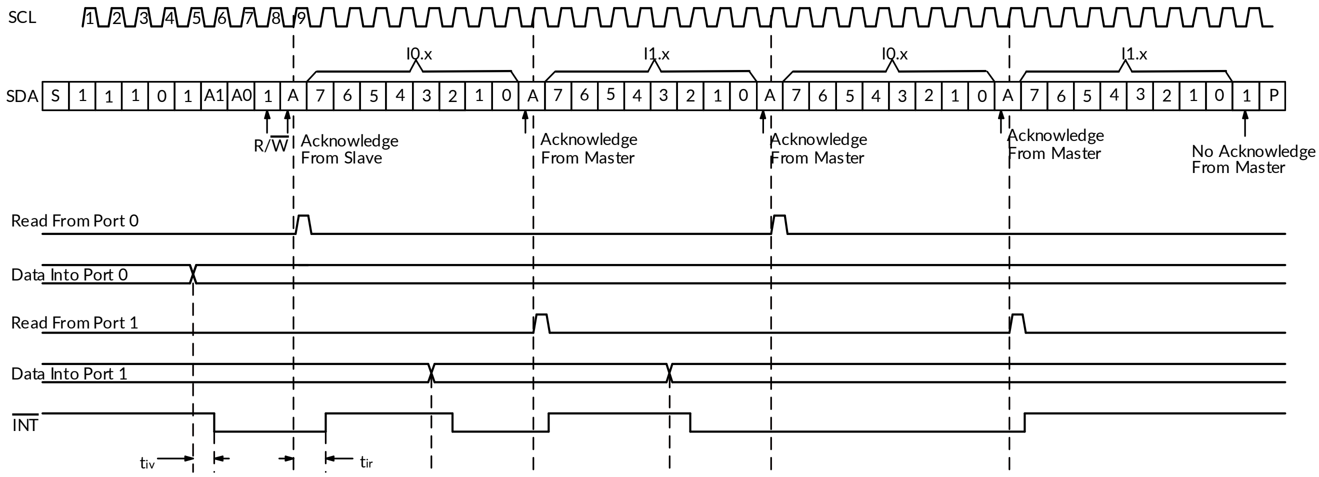


Figure 12. Read from Register

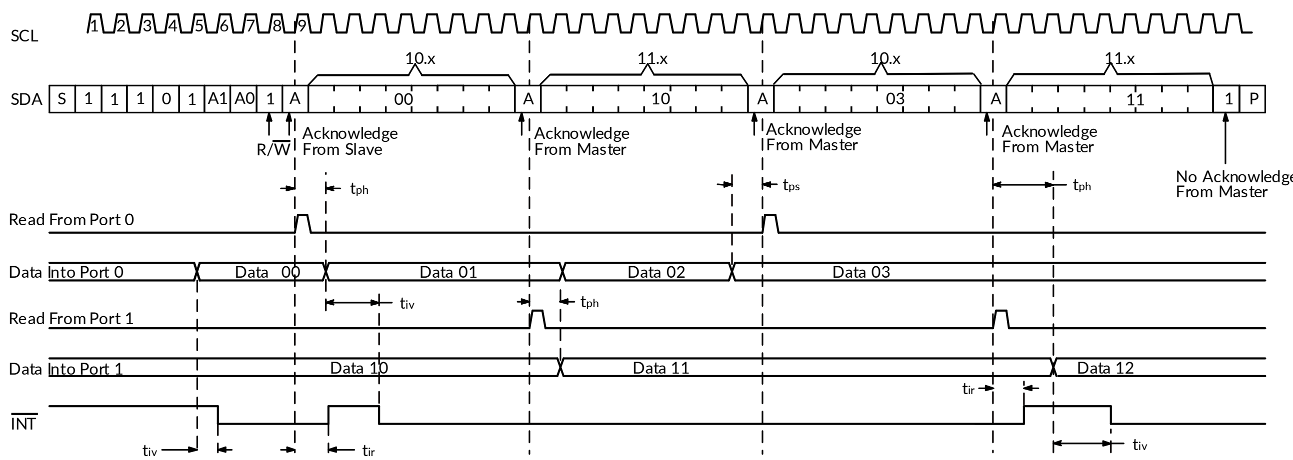
After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. Figure 13 and Figure 14 show two different scenarios of Read Input Port Register.



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 13. Read Input Port Register, Scenario 1



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

Figure 14. Read Input Port Register, Scenario 2

9.5.2 Device Address

Figure 15 shows the address byte of the RS29539.

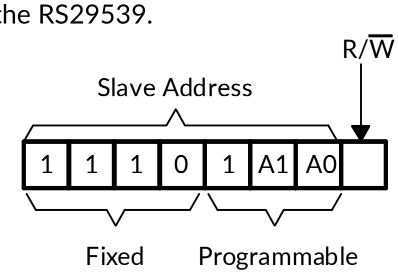


Figure 15. RS29539 Address

Table 2 shows the address reference of the RS29539.

Table 2. Address Reference

INPUTS		I²C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 0×74 (hexadecimal)
L	H	117 (decimal), 0x75 (hexadecimal)
H	L	118 (decimal), 0x76 (hexadecimal)
H	H	119 (decimal), 0x77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.
Note that the I^2C addresses shown above are the 7-bit, right-justified hexadecimal values.

9.5.3 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte shown in Table 3 that is stored in the control register in the RS29539. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.
When a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 16 shows the control register bits.

0	0	0	0	0	B2	B1	B0

Figure 16. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

9.6 Register Maps

9.6.1 Register Descriptions

The Input Port registers (registers 0 and 1) shown in Table 4 reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port registers are accessed next.

Table 4. Registers 0 and 1 (Input Port Registers)

Bit	**I0.7**	**I0.6**	**I0.5**	**I0.4**	**I0.3**	**I0.2**	**I0.1**	**I0.0**
Default	X	X	X	X	X	X	X	X
Bit	**I1.7**	**I1.6**	**I1.5**	**I1.4**	**I1.3**	**I1.2**	**I1.1**	**I1.0**
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shown in Table 5 show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Registers 2 and 3 (Output Port Registers)

Bit	**O0.7**	**O0.6**	**O0.5**	**O0.4**	**O0.3**	**O0.2**	**O0.1**	**O0.0**
Default	1	1	1	1	1	1	1	1
Bit	**O1.7**	**O1.6**	**O1.5**	**O1.4**	**O1.3**	**O1.2**	**O1.1**	**O1.0**
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) shown in Table 6 allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding pin's original polarity is retained.

Table 6. Registers 4 and 5 (Polarity Inversion Registers)

Bit	**N0.7**	**N0.6**	**N0.5**	**N0.4**	**N0.3**	**N0.2**	**N0.1**	**N0.0**
Default	0	0	0	0	0	0	0	0
Bit	**N1.7**	**N1.6**	**N1.5**	**N1.4**	**N1.3**	**N1.2**	**N1.1**	**N1.0**
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) shown in Table 7 configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Registers 6 and 7 (Configuration Registers)

Bit	**C0.7**	**C0.6**	**C0.5**	**C0.4**	**C0.3**	**C0.2**	**C0.1**	**C0.0**
Default	1	1	1	1	1	1	1	1
Bit	**C1.7**	**C1.6**	**C1.5**	**C1.4**	**C1.3**	**C1.2**	**C1.1**	**C1.0**
Default	1	1	1	1	1	1	1	1

10 APPLICATION AND IMPLEMENTATION

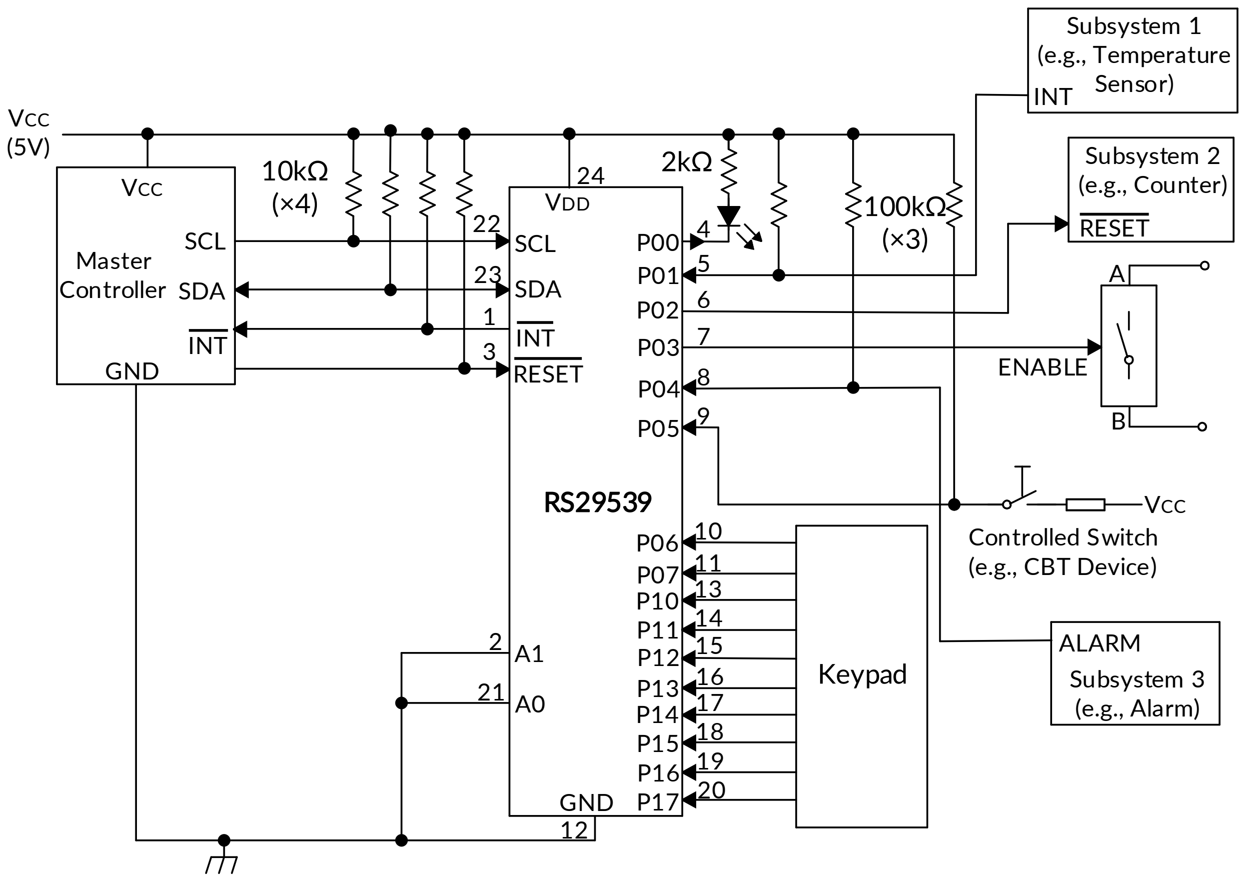
Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Applications of the RS29539 has this device connected as a slave to an I^{2}C master (processor), and the I^{2}C bus may contain any number of other slave devices. The RS29539 is typically in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.
IO Expanders such as the RS29539 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

10.2 Typical Application

Figure 17 shows an application in which the RS29539 can be used.



A. Device address is configured as 1110100 for this example.
B. P00, P02, and P03 are configured as outputs.
C. P01 and P04 to P17 are configured as inputs.
D. Pin numbers shown are for the TSSOP24 package.

Figure 17. Application Schematic

10.2.1 Design Requirements

10.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with this device, it is important that the Recommended Operating Conditions not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in Thermal Information table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

10.2.1.2 Minimizing I_{CC} When I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in Figure 17. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in the Electrical Characteristics table shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption.

Figure 18 shows a high-value resistor in parallel with the LED. Figure 19 shows V_{CC} less than the LED supply voltage by at least 1.2V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

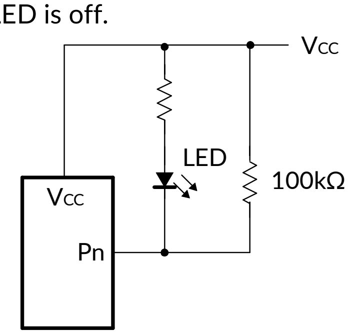


Figure 18. High-Value Resistor in Parallel With LED

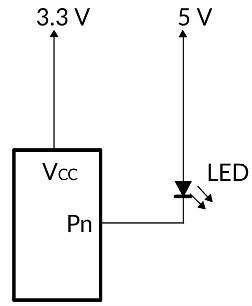


Figure 19. Device Supplied by Lower Voltage

10.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,max}$), and I_{OL} as shown in Equation 5.

$$R_{P(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \qquad (5)$$

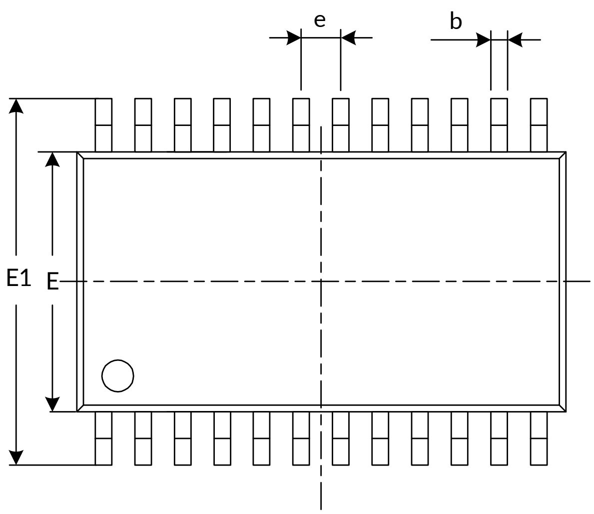
The maximum pull-up resistance is a function of the maximum rise time, tr (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

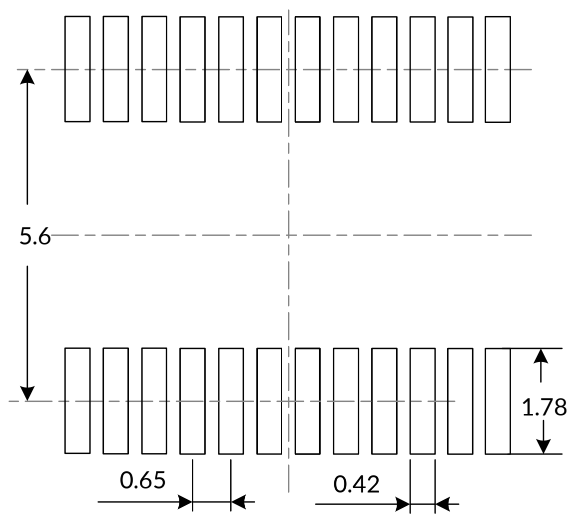
$$R_{P(max)} = \frac{t_r}{0.8473 \times C_b} \qquad (6)$$

The maximum bus capacitance for an I^2C bus must not exceed 400pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the RS29539, C_i for SCL or C_{IO} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

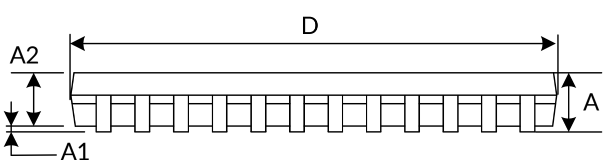
11 PACKAGE OUTLINE DIMENSIONS

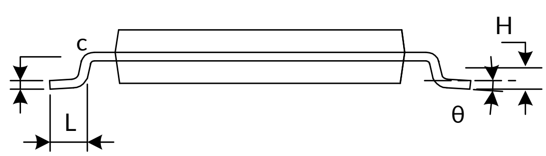
TSSOP24 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





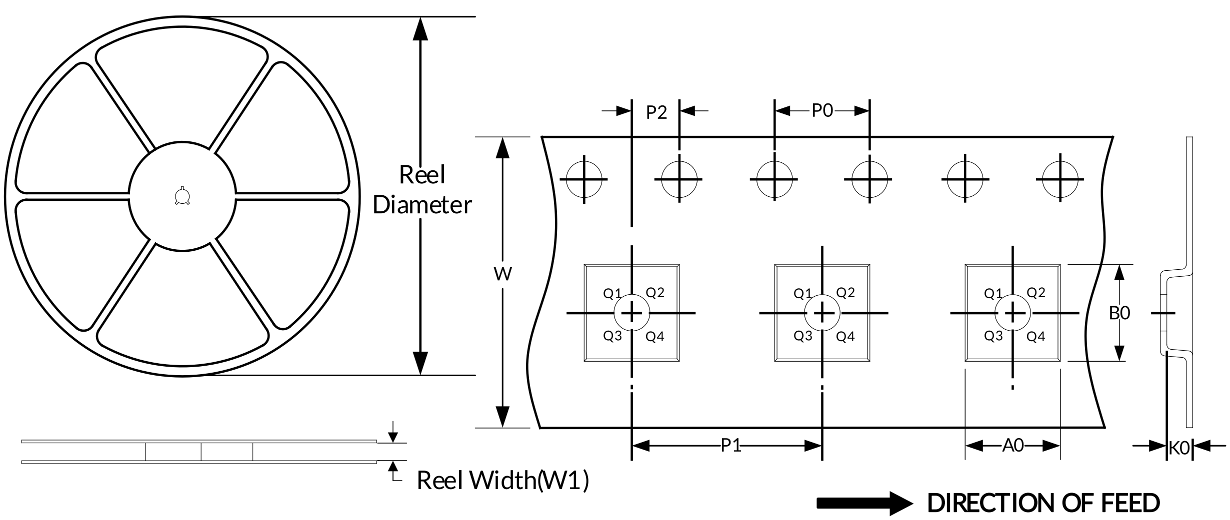
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.200	0.290	0.008	0.011
c	0.130	0.170	0.005	0.007
D (1)	7.700	7.900	0.303	0.311
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
L	0.450	0.750	0.018	0.030
H	0.250 (TYP)		0.010 (TYP)	
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP24	13"	16.4	6.95	8.30	1.60	4.0	8.0	2.0	16.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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