Octal Buffers and Line Drivers With 3-State Outputs

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Power-Supply Range: 4.5V to 5.5V**
- **3-State Outputs Drive Bus Lines**
- **Low Power Consumption: 40μA I_{CC}(Max)**
- **TTL Input are Compatible**
- **±24mA Output Drive at 5V**
- **Low Input Current of 2μA Max**
- **Extended Temperature: -40°C to 125°C**
- **Micro SIZE PACKAGES: TSSOP20**

2 APPLICATIONS

- **HEV/EV Inverter & Motor Control**
- **HEV Battery Management System**

3 DESCRIPTIONS

The RS541T-Q1 is an 8-bit non-inverting buffer/line driver with 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A High on $\overline{OE}$ causes the associated outputs to assume a high-impedance OFF-state.

Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

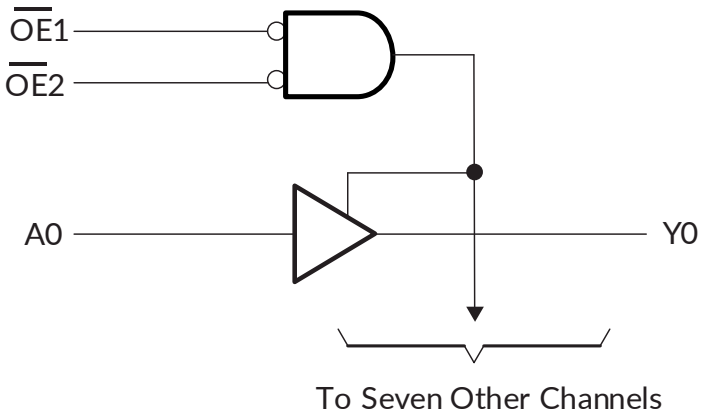
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS541T-Q1	TSSOP20	6.50mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



Function Table

INPUTS			OUTPUT
$\overline{OE}1$	$\overline{OE}2$	A PORT	Y PORT
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

NOTE:
H=HIGH voltage level
L=LOW voltage level
X=Don't care
Z=High impedance OFF-state

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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/03/14	Preliminary version completed
A.1	2024/08/05	Initial version completed

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS541T-Q1	RS541TXTSS20-Q1	-40°C ~125°C	TSSOP20	Plating Sn	MSL1-260°-Unlimited	RS541T	Tape and Reel,4000

NOTE:

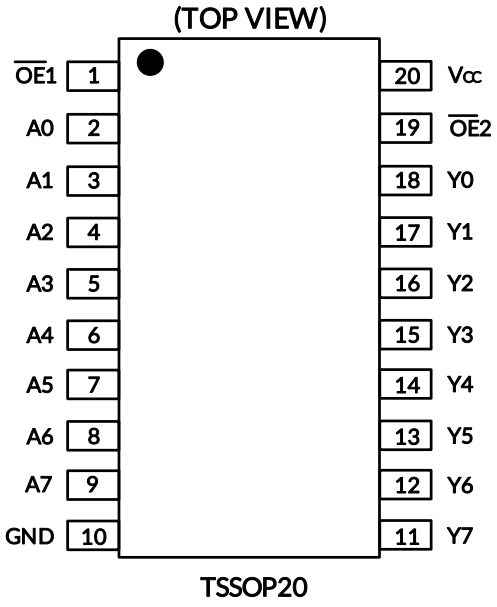
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

7 PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
TSSOP20			
1	$\overline{OE}1$	I	Output Enable (Active Low). Pull $\overline{OE}1$ high to place all outputs in 3-state mode.
2	A0	I	Data Input
3	A1	I	Data Input
4	A2	I	Data Input
5	A3	I	Data Input
6	A4	I	Data Input
7	A5	I	Data Input
8	A6	I	Data Input
9	A7	I	Data Input
10	GND	G	Ground.
11	Y7	O	Data Output
12	Y6	O	Data Output
13	Y5	O	Data Output
14	Y4	O	Data Output
15	Y3	O	Data Output
16	Y2	O	Data Output
17	Y1	O	Data Output
18	Y0	O	Data Output
19	$\overline{OE}2$	I	Output Enable (Active Low). Pull $\overline{OE}2$ high to place all outputs in 3-state mode.
20	V_{CC}	P	Supply voltage: 4.5V≤V_{CC}≤5.5V

(1) I=input, O=output, P=power, G= Ground.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage Range		-0.5	6.5	V
V_I(2)	Input Voltage Range		-0.5	6.5	V
V_O(2)(3)	Output Voltage Range		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	Vo<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	TSSOP20		40	°C/W
T_J	Junction Temperature (5)		-40	150	°C
T_{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±1000	V
		Latch-Up (LU), per AEC Q100-004	±100	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CC} is the supply voltage associated with the input port and output port. (1)(2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
High-Level Input Voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=4.5V to 5.5V			0.8	V
Input Voltage	V_I		0		V_{CC}	V
Output Voltage	V_O		0		V_{CC}	V
High-Level Output Current	I_{OH}	V_{CC}=4.5V to 5.5V			-24	mA
Low-Level Output Current	I_{OL}	V_{CC}=4.5V to 5.5V			24	mA
Input transition rise or fall rate	Δt/Δv	V_{CC}=4.5V to 5.5V			8	ns/V
Operating free-air Temperature	T_A		-40		125	°C

(1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CC} or GND) to ensure proper device operation and minimize power.
(2) All unused control inputs must be held at V_{CC} or GND to ensure proper device operation and minimize power consumption.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full = -40°C to 125°C, unless otherwise noted).

PARAMETER	CONDITIONS	V_{CC}	TEMP	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OH}	I_{OH} = -50μA	4.5V	Full	4.4			V
		5.5V		5.4			
	I_{OH} = -24mA	4.5V		3.76			
		5.5V		4.76			
	I_{OH} = -50mA	5.5V		3.85			
V_{OL}	I_{OL} = 50μA	4.5V				0.1	V
		5.5V				0.1	
	I_{OL} = 24mA	4.5V				0.73	
		5.5V				0.69	
	I_{OL} = 50mA	5.5V				1.65	
I_I	V_I = V_{CC} or GND	5.5V	+25°C			±1	μA
			Full			±2	
I_{off}	V_I or V_O= 0 to 5.5V	0V	+25°C			±1	μA
			Full			±2	
I_{OZ} (3)	V_O = V_{CC} or GND, V_I = V_{IH} or V_{IL}	5.5V	+25°C			±1	μA
			Full			±2.5	
I_{CC}	V_I = V_{CC} or GND (4) I_O = 0	5.5V	+25°C			4	μA
			Full			40	
ΔI_{CC}	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5V	+25°C		0.6		mA
			Full			1.5	
C_I	V_I = V_{CC} or GND	5V	+25°C		3.3		pF
C_O	V_O = V_{CC} or GND	5V	+25°C		5.5		pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) Hold all unused data inputs of the device at V_{CCI} or GND to assure proper device operation.

8.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C (1)			T_A = -40 ~ 125°C (1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	An	Yn	2.2	4.8	7.9	2.1		9.1	ns
t_{PHL}			2.1	4.7	7.8	2.0		8.8	
t_{PHZ}	$\overline{OE}$	Yn	1.8	4.3	7.6	1.7		8.2	ns
t_{PLZ}			2.3	5.1	8.2	2.1		9.7	
t_{PZH}	$\overline{OE}$	Yn	2.7	6.1	11.8	1.7		12.8	ns
t_{PZL}			1.1	3.1	5.5	0.8		9.3	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.6 Operating Characteristics

T_A=25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 5V	UNIT
			TYP	
C_{pd}(1)	Power dissipation capacitance per buffer/driver	C_L = 50 pF, f = 1 MHz	39	pF

(1) Power dissipation capacitance per transceiver.

8.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, V_{CC}=5.5V, unless otherwise noted.

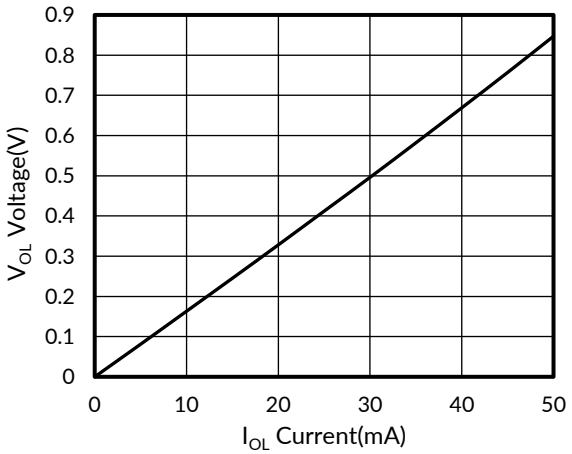


Figure 1. Voltage vs Current

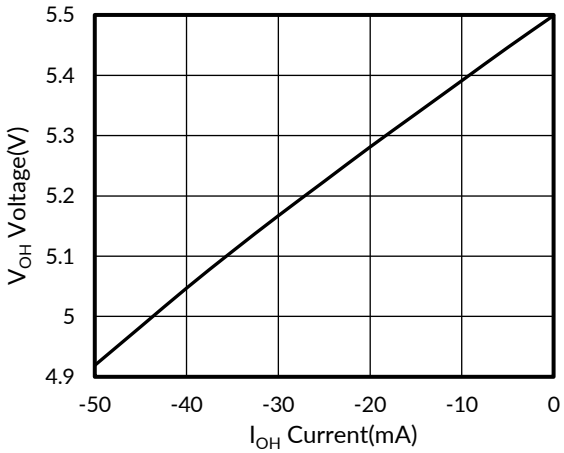
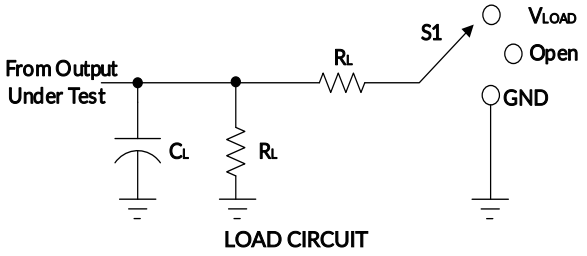


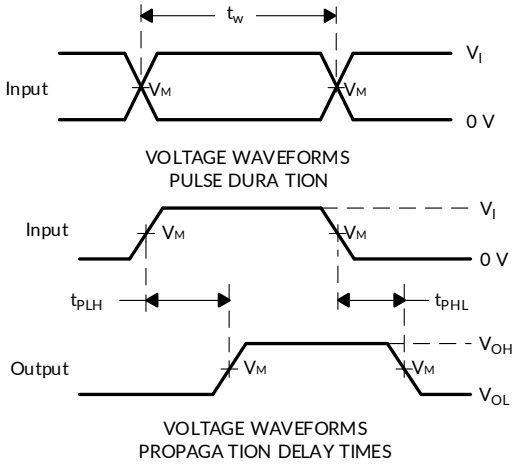
Figure 2. Voltage vs Current

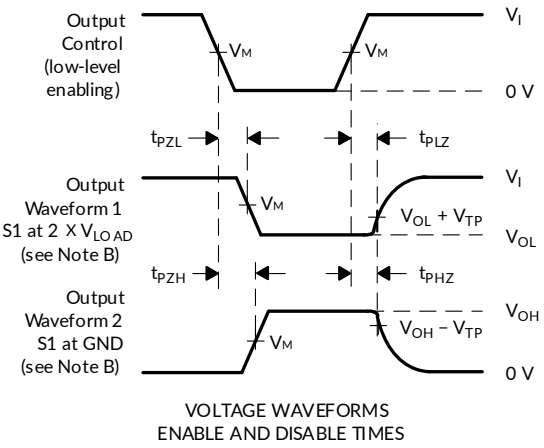
9 PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_M	C_L	R_L	V_{TP}
5V±0.5V	2.7V	1.5V	15pF	2kΩ	0.3V





NOTES: A.CL includes probe and jig capacitance.
B.Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50Ω, dv/dt≥1V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

10 DETAILED DESCRIPTION

10.1 Overview

The RS541T-Q1 is an 8-bit non-inverting buffer/line driver with 3-state outputs. The device features two output enables ($\overline{OE}1$ and$\overline{OE}2$). A High on $\overline{OE}$ causes the associated outputs to assume a high-impedance OFF-state. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor, the minimum value of the resistor is determined by the current-sinking capability of the driver.

11 POWER SUPPLY RECOMMENDATIONS

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 LAYOUT

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

12.2 Layout Example

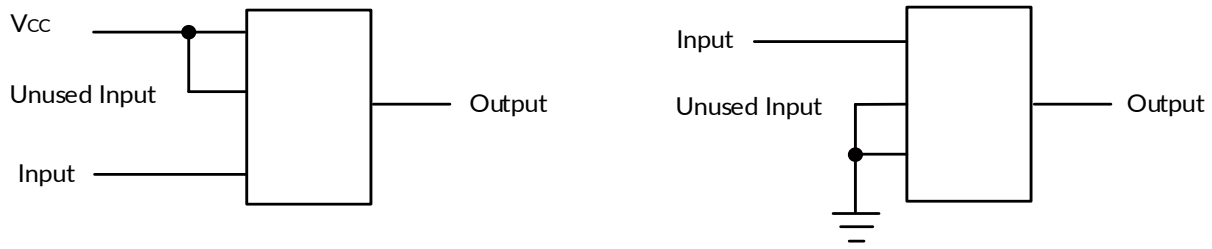
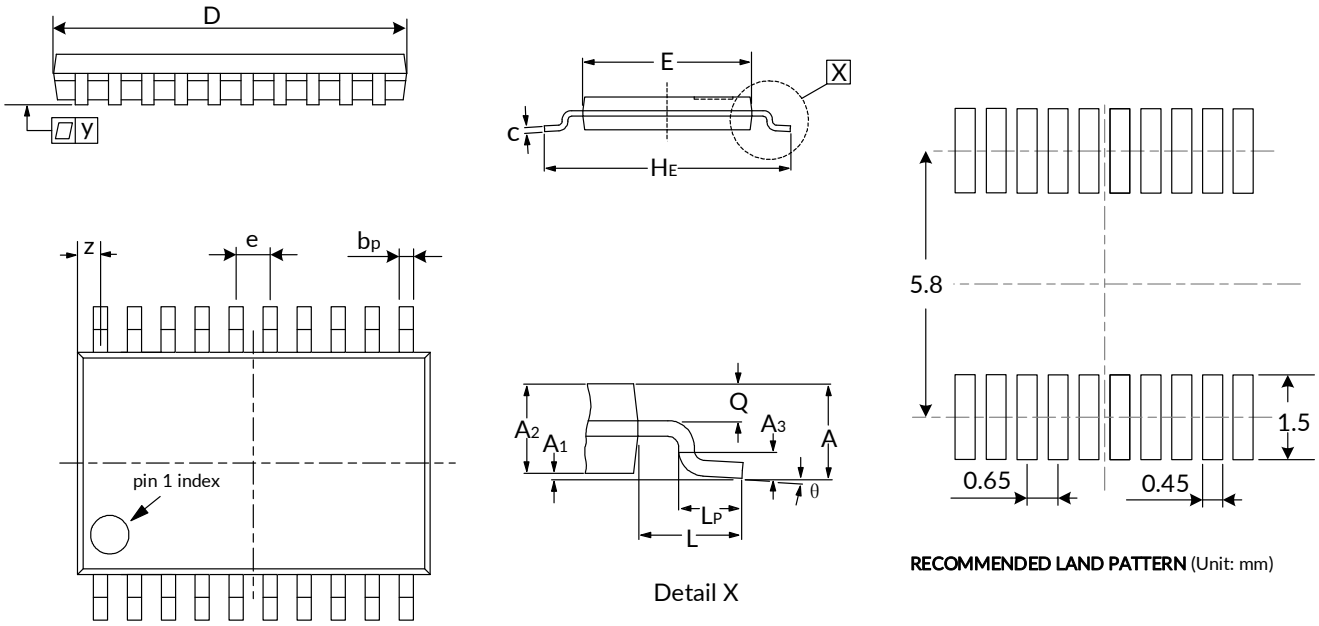


Figure 4. Layout Diagram

13 PACKAGE OUTLINE DIMENSIONS

TSSOP20 (2)



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.100		0.043
A_1	0.050	0.150	0.002	0.006
A_2	0.800	0.950	0.031	0.037
A_3	0.250		0.010	
b_p	0.190	0.300	0.007	0.012
c	0.100	0.200	0.004	0.008
D (1)	6.400	6.600	0.251	0.260
E (1)	4.300	4.500	0.169	0.177
H_E	6.200	6.600	0.244	0.260
e	0.650		0.026	
L	1.000		0.039	
L_P	0.500	0.750	0.020	0.030
Q	0.300	0.400	0.012	0.016
Z	0.200	0.500	0.008	0.020
y	0.100		0.004	
θ	0°	8°	0°	8°

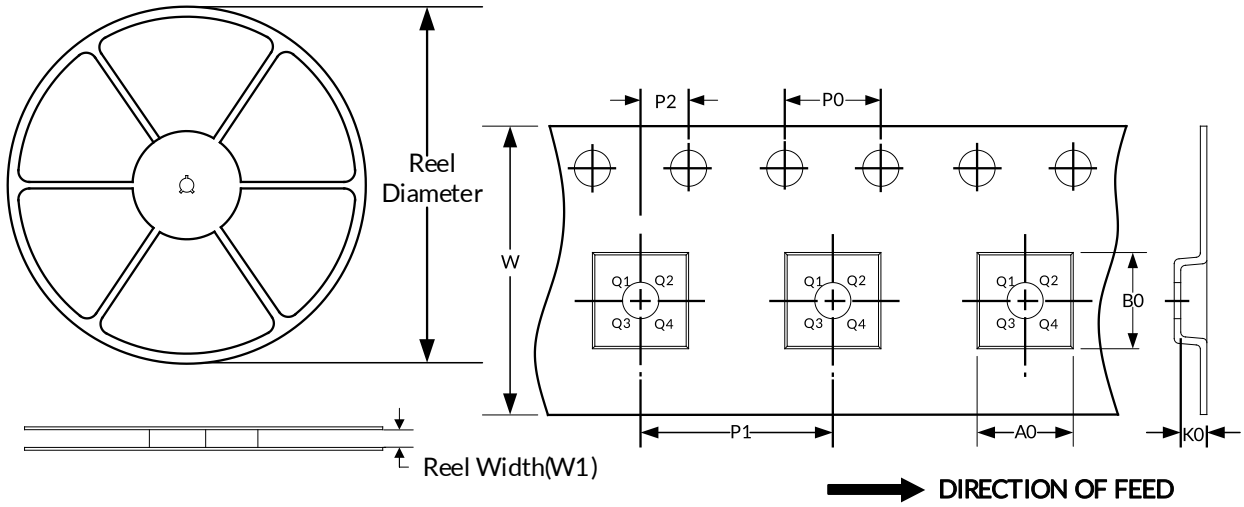
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP20	13”	12.4	6.75	6.95	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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