4:1, 2-Channel Multiplexers
with Injection Current Control

1 FEATURES

- **Injection Current Control**
- **Back-Powering Protection**
  – No ESD Diode Path to V_{DD}
- **Supply Range: 1.6V to 5.5V**
- **1.8 V Logic Compatible**
- **Fail-Safe Logic**
- **Break-Before-Make Switching**
- **Rail-to-Rail Operation**
- **Extended Industrial Temperature Range: -40°C to 125°C**
- **PACKAGES: TSSOP16, QFN2.5X3.5-16**

2 APPLICATIONS

- **Analog and Digital Multiplexing and Demultiplexing**
- **Diagnostics and Monitoring**
- **Body Control Modules**
- **Battery Management Systems (BMS)**
- **HVAC Control Module**
- **Automotive Head Unit**
- **Telematics**
- **On-Board (OBC) and Wireless Charging**

3 DESCRIPTIONS

The RMUX1309 is a 4:1, 2-channel multiplexers. The devices support bidirectional analog and digital signals on the source (S_X) and drain (D_X) pins ranging from GND to V_{DD}.

The RMUX1309 devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows signals on disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. Additionally, the RMUX1309 devices do not have an internal diode path to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the supply rail.

All logic inputs have 1.8V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating with a valid supply voltage. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RMUX1309	TSSOP16	5.00mm×4.40mm
	QFN2.5X3.5-16	2.50mm×3.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/11/15	Preliminary version completed
A.1	2025/03/31	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING(2)	MSL(3)	PACKAGE OPTION
RMUX1309	RMUX1309XTSS16	-40°C ~125°C	TSSOP16	RMUX1309	MSL3	Tape and Reel,4000
	RMUX1309XTQW16	-40°C ~125°C	QFN2.5X3.5-16	RMUX1309	MSL3	Tape and Reel,5000

NOTE:

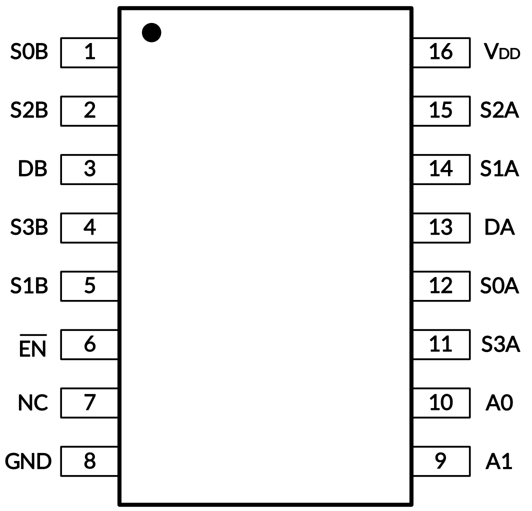
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

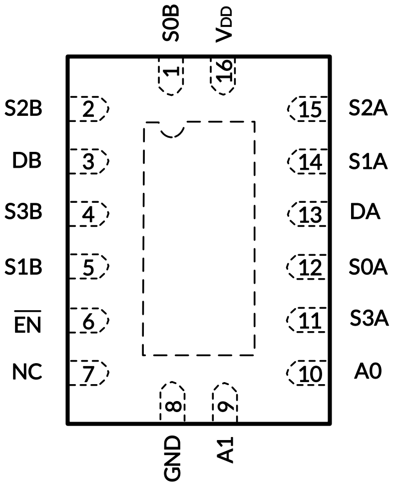
6 PIN CONFIGURATION AND FUNCTIONS

(TOP VIEW)



TSSOP16

(TOP VIEW)



QFN2.5X3.5-16

PIN DESCRIPTION

NAME	PIN	TYPE (1)	DESCRIPTION (2)
	TSSOP16/ QFN2.5X3.5-16		
S0B	1	I/O	Source pin 0 of mux B. Can be an input or output.
S2B	2	I/O	Source pin 2 of mux B. Can be an input or output.
DB	3	I/O	Drain pin (common) of mux B. Can be an input or output.
S3B	4	I/O	Source pin 3 of mux B. Can be an input or output.
S1B	5	I/O	Source pin 1 of mux B. Can be an input or output.
$\overline{EN}$	6	I	Active low logic input. When this pin is high, all switches are turned off. When this pin is low, the A[1:0] address inputs determine which switch is turned on.
NC	7	Not Connected	Not internally connected.
GND	8	P	Ground (0 V) reference.
A1	9	I	Address line 1. Controls the switch configuration as listed in Table 1.
A0	10	I	Address line 0. Controls the switch configuration as listed in Table 1.
S3A	11	I/O	Source pin 3 of mux A. Can be an input or output.
S0A	12	I/O	Source pin 0 of mux A. Can be an input or output.
DA	13	I/O	Drain pin (common) of mux A. Can be an input or output.
S1A	14	I/O	Source pin 1 of mux A. Can be an input or output.
S2A	15	I/O	Source pin 2 of mux A. Can be an input or output.
V_{DD}	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
Thermal pad		-	Exposed thermal pad with conductive die attached. No requirement to solder this pad. If connected, then it should be left floating or tied to GND.

(1) I=Input, O=Output, I/O=Input and Output, P=Power.
(2) For what to do with unused pins, refer to Section 9.4.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{DD}	Supply voltage		-0.5	6.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1)		-0.5	6.5	
V_S or V_D	Source or drain voltage (S_X, D_X)		-0.5	V_{DD}+0.5	
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, A0, A1)		-50	50	mA
I_S or $I_{D\ (CONT)}$	Continuous current through switch (S_X, D_X pins)		-50	50	
I_{GND}	Continuous current through GND		-100	100	
P_{tot}	Total power dissipation			500	mW
$θ_{JA}$	Package thermal impedance (4)	TSSOP16		125	°C/W
		QFN2.5X3.5-16		65	
T_J	Junction Temperature (5)			150	°C
T_{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(3) All voltages are with respect to ground, unless otherwise specified.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC-Q100-002-REV-E (2013)	±2000	V
		Charged-Device Model (CDM), per AEC-Q100-011 REV-D (2019)	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply voltage	1.6	5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (S_X, D_X)	0	V_{DD}	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1)	0	5.5	V
I_S or $I_{D\ (CONT)}$	Continuous current through switch (S_X, D_X pins)	-50	50	mA
I_{OK}	Current per input into source or drain pins when signal voltage exceeds recommended operating voltage (1)	-50	50	mA
I_{INJ}	Injected current into single off switch input	-50	50	mA
I_{INJ_ALL}	Total injected current into all off switch inputs combined	-100	100	mA
T_A	Ambient temperature	-40	125	°C

(1) If source or drain voltage exceeds V_{DD}, or goes below GND, the pin will be shunted to GND through an internal FET, the current must be limited within the specified value. If $V_{signal} > V_{DD}$ or if $V_{signal} <$ GND.

7.4 Electrical Characteristics

At specified V_{DD} ±10%. Typical values measured at nominal V_{DD}.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{DD}	TEMP	MIN	TYP	MAX	UNIT
ANALOG SWITCH								
R_{ON}	On-state switch resistance	V_S = 0V to V_{DD} I_{SD} = 0.5mA	1.8V	25°C		800	1500	Ω
				FULL			1700	
			2.5V	25°C		230	600	
				FULL			670	
			3.3V	25°C		140	330	
				FULL			370	
			5V	25°C		95	200	
				FULL			270	
ΔR_{ON}	On-state switch resistance matching between inputs	V_S = V_{DD} / 2 I_{SD} = 0.5mA	1.8V	FULL		35	52	Ω
			2.5V	FULL		10	22	
			3.3V	FULL		3	15	
			5V	FULL		2	14	
$I_{S(OFF)}$ $I_{D(OFF)}$	Off state leakage current	Switch Off V_D or V_S = 0 to V_{DD}	1.6V to 5.5V	FULL		±0.1	±3	µA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on state leakage current	Switch On V_D or V_S = 0 to V_{DD}	1.6V to 5.5V	FULL		±0.1	±3	µA
C_{SOFF}	Source off capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8V	25°C		4		pF
			2.5V			4		
			3.3V			4		
			5V			4		
C_{DOFF}	Drain off capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8V	25°C		6		pF
			2.5V			6		
			3.3V			6		
			5V			6		
C_{SON} C_{DON}	On capacitance	V_S = V_{DD} / 2 f = 1 MHz	1.8V	25°C		12		pF
			2.5V			12		
			3.3V			12		
			5V			12		
POWER SUPPLY								
I_{DD}	V_{DD} supply current	Logic inputs = 0V or V_{DD}	1.6V to 5.5V	25°C		0.1	1	µA
				FULL			4	

7.5 Logic and Dynamic Characteristics

At specified V_{DD} ±10%. Typical values measured at nominal V_{DD} and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{DD}	TEMP	MIN	TYP	MAX	UNIT
LOGIC INPUTS ($\overline{EN}$, A0, A1)								
V_{IH}	Input logic high		1.8V	FULL	1.1			V
			2.5V		1.2			
			3.3V		1.25			
			5V		1.4			
V_{IL}	Input logic low		1.8V	FULL			0.55	V
			2.5V				0.65	
			3.3V				0.75	
			5V				0.9	
I_{IN}	Input leakage current	V_{IN} = 0 V or V_{DD}	1.6V to 5.5V	25°C		±0.1	±1	μA
				FULL			±2	
C_{IN}	Logic input capacitance	V_{LOGIC} = 0 V, 1.8 V, V_{DD} f = 1 MHz	1.6V to 5.5V	25°C		6.5		pF
DYNAMIC CHARACTERISTICS								
Q_{INJ}	Charge Injection	$V_S = V_{DD}$ / 2 R_S = 0 Ω, C_L = 100 pF	1.8V	25°C		-0.5		pC
			2.5V			-0.5		
			3.3V			-1		
			5V			-6.5		
O_{ISO}	Off Isolation	$V_{BIAS} = V_{DD}$ / 2 V_S = 200mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8V	25°C		−110		dB
			2.5V			−110		
			3.3V			−110		
			5V			−110		
O_{ISO}	Off Isolation	$V_{BIAS} = V_{DD}$ / 2 V_S = 200mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8V	25°C		−90		dB
			2.5V			−90		
			3.3V			−90		
			5V			−90		
X_{TALK}	Crosstalk	$V_{BIAS} = V_{DD}$ / 2 V_S = 200mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8V	25°C		−110		dB
			2.5V			−110		
			3.3V			−110		
			5V			−110		
X_{TALK}	Crosstalk	$V_{BIAS} = V_{DD}$ / 2 V_S = 200mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8V	25°C		−90		dB
			2.5V			−90		
			3.3V			−90		
			5V			−90		
BW	Bandwidth	$V_{BIAS} = V_{DD}$ / 2 V_S = 200mVpp R_L = 50 Ω, C_L = 5 pF	1.8V	25°C		185		MHz
			2.5V			200		
			3.3V			210		
			5V			220		

7.6 Timing Characteristics

At specified V_{DD} ±10%. Typical values measured at nominal V_{DD}.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{DD}	TEMP	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS								
t_{PD}	Propagation delay	C_L = 50pF S_X to D_X, D_X to S_X	1.8V	25°C		15	31	ns
				FULL			48	
			2.5V	25°C		10	17	
				FULL			20	
			3.3V	25°C		6	14	
				FULL			23	
			5V	25°C		5	8	
				FULL			18	
		C_L = 15pF	5V	25°C		3	6	
				FULL			10	
t_{TRAN}	Transition-time between inputs	R_L = 10kΩ, C_L = 50pF A_X to D_X, A_X to S_X	1.8V	25°C		71	104	ns
				FULL			150	
			2.5V	25°C		45	66	
				FULL			95	
			3.3V	25°C		37	53	
				FULL			75	
			5V	25°C		32	46	
				FULL			63	
		R_L = 10kΩ, C_L = 15pF	5V	25°C		30	44	
				FULL			52	
$t_{ON(EN)}$	Turn on-time from enable	R_L = 10kΩ, C_L = 50pF EN to D_X, EN to S_X	1.8V	25°C		78	99	ns
				FULL			142	
			2.5V	25°C		50	63	
				FULL			96	
			3.3V	25°C		41	51	
				FULL			77	
			5V	25°C		36	45	
				FULL			69	
		R_L = 10kΩ, C_L = 15pF	5V	25°C		35	43	
				FULL			65	
$t_{OFF(EN)}$	Turn off-time from enable	R_L = 10kΩ, C_L = 50pF EN to D_X, EN to S_X	1.8V	25°C		110	130	ns
				FULL			175	
			2.5V	25°C		84	100	
				FULL			135	
			3.3V	25°C		73	88	
				FULL			115	
			5V	25°C		41	50	
				FULL			65	
		R_L = 10kΩ, C_L = 15pF	5V	25°C		35	45	
				FULL			55	

t_{BBM}	Break before make time	R_L = 10kΩ, C_L = 15pF S_X to D_X, D_X to S_X	1.8V	FULL		46	82	ns
			2.5V			42	75	
			3.3V			35	60	
			5V			32	65	

7.7 Injection Current Coupling

At specified V_{DD} ±10%. Typical values measured at nominal V_{DD} and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS		V_{DD}	TEMP	MIN	TYP	MAX	UNIT
ΔVOUT	Maximum shift of output voltage of enabled analog input	$R_S \le 3.9k\Omega$, $V_{IN} = V_{DD}/2$	0≤ I ≤ 1mA	1.8V	FULL		0.2	1	mV
				3.3V			0.1	1	
				5V			0.05	1	
		$R_S \le 3.9k\Omega$, $V_{IN} = V_{DD}/2$	0≤ I ≤ 10mA	1.8V	FULL		0.3	4	
				3.3V			0.15	4	
				5V			0.1	4	
		$R_S \le 20k\Omega$, $V_{IN} = V_{DD}/2$	0≤ I ≤ 1mA	1.8V	FULL		0.2	2	
				3.3V			0.1	2	
				5V			0.05	2	
		$R_S \le 20k\Omega$, $V_{IN} = V_{DD}/2$	0≤ I ≤ 10mA	1.8V	FULL		0.25	15	
				3.3V			0.15	15	
				5V			0.1	15	
ΔVOUT	Maximum shift of output voltage of enabled analog input	$R_S \le 3.9k\Omega$, $V_{IN} = V_{DD}/2$	-1mA ≤ I ≤ 0	1.8V	FULL		3	50	mV
				3.3V			0.7	1	
				5V			0.5	1	
		$R_S \le 3.9k\Omega$, $V_{IN} = V_{DD}/2$	-10mA ≤ I ≤ 0	1.8V	FULL		32	50	
				3.3V			5	8	
				5V			3.5	8	
		$R_S \le 20k\Omega$, $V_{IN} = V_{DD}/2$	-1mA ≤ I ≤ 0	1.8V	FULL		4	50	
				3.3V			0.7	2	
				5V			0.5	2	
		$R_S \le 20k\Omega$, $V_{IN} = V_{DD}/2$	-10mA ≤ I ≤ 0	1.8V	FULL		40	50	
				3.3V			5.8	15	
				5V			3.5	15	

7.8 Application Information

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = 25°C, V_{DD} = 5 V (unless otherwise noted).

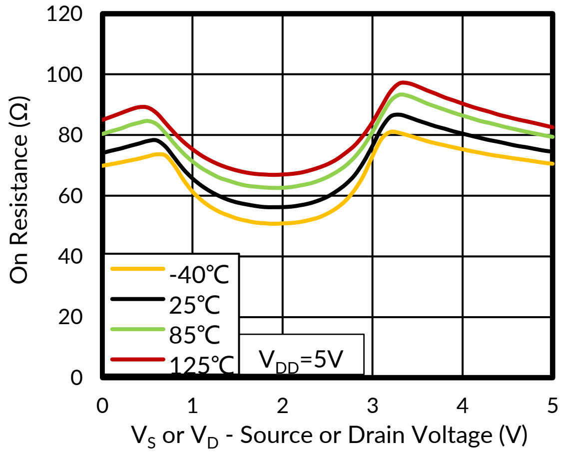


Figure 1. On-Resistance vs Temperature

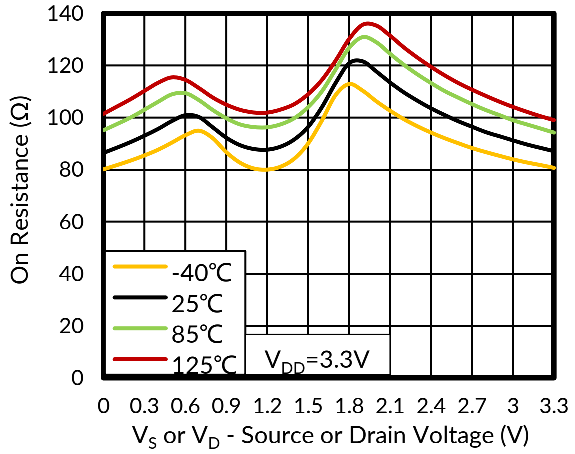


Figure 2. On-Resistance vs Temperature

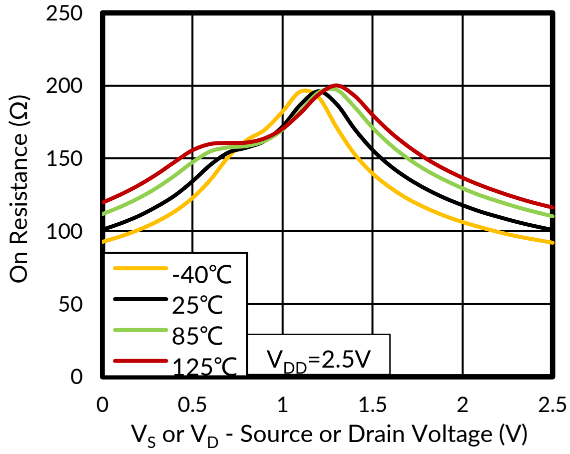


Figure 3. On-Resistance vs Temperature

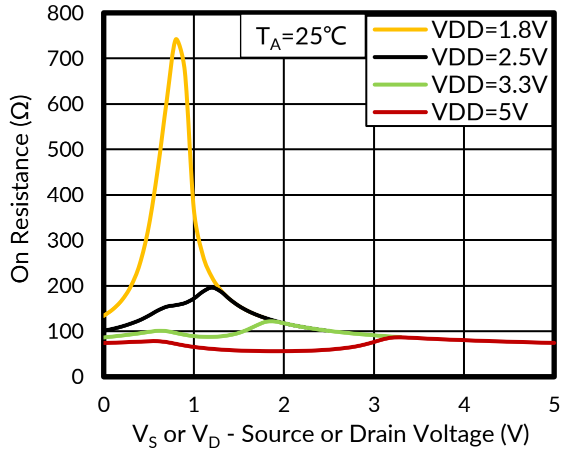


Figure 4. On-Resistance vs Source or Drain Voltage

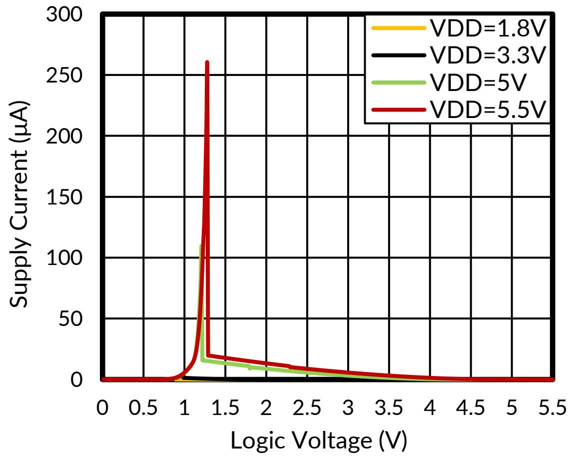


Figure 5. Supply Current vs Logic Voltage

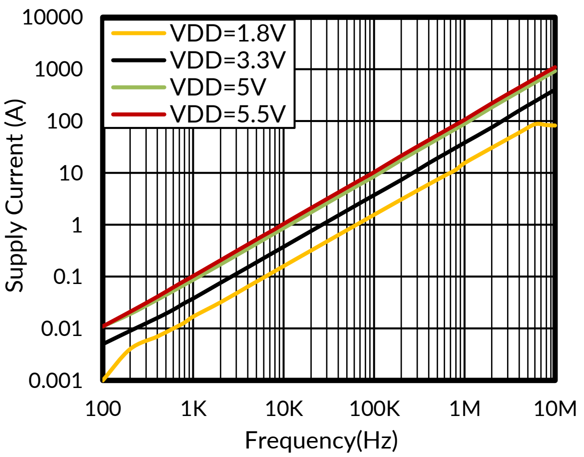


Figure 6. Supply Current vs Input Switching Frequency

Application Information

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, V_{DD} = 5 V (unless otherwise noted).

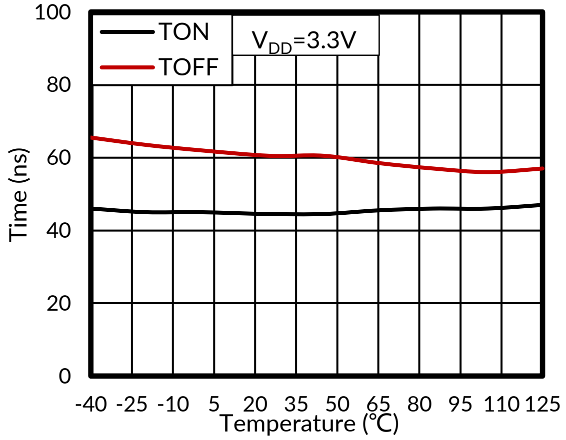


Figure 7. T_{on} and T_{off} vs Temperature

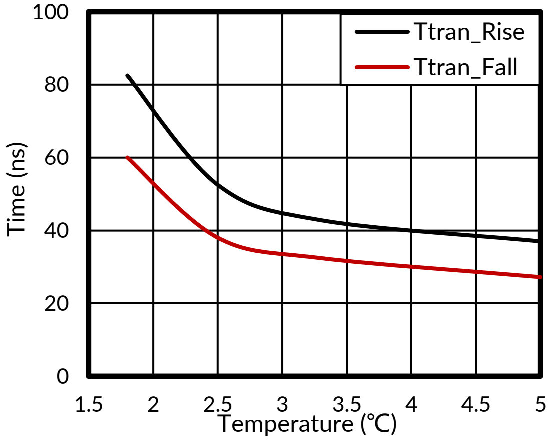


Figure 8. $T_{TRANSITION}$ vs Supply Voltage

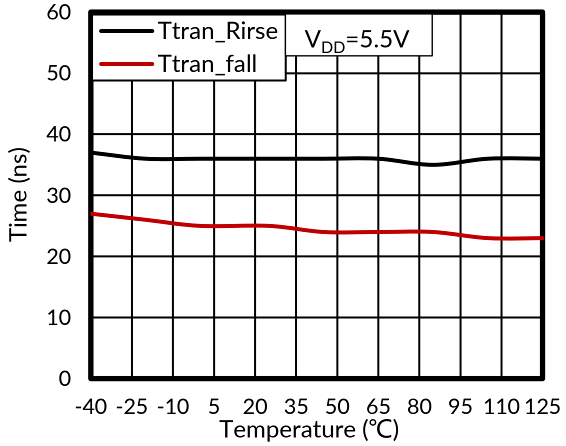


Figure 9. $T_{TRANSITION}$ vs Temperature

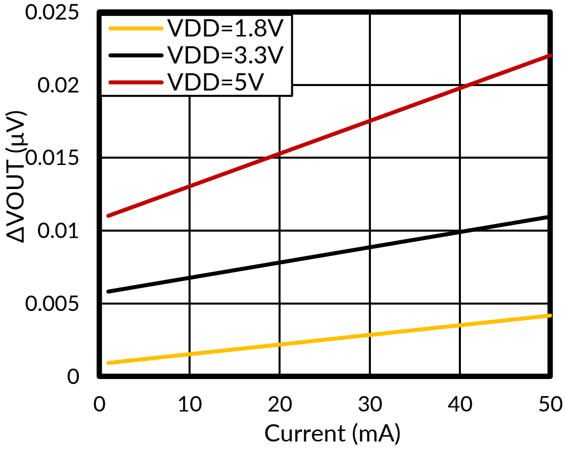


Figure 10. Injection Current vs Maximum Output Voltage Shift

8 PARAMETER MEASUREMENT INFORMATION

8.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (S_X) and drain (D_X) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown below. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed as shown in Figure 11 with $R_{ON} = V / I_{SD}$:

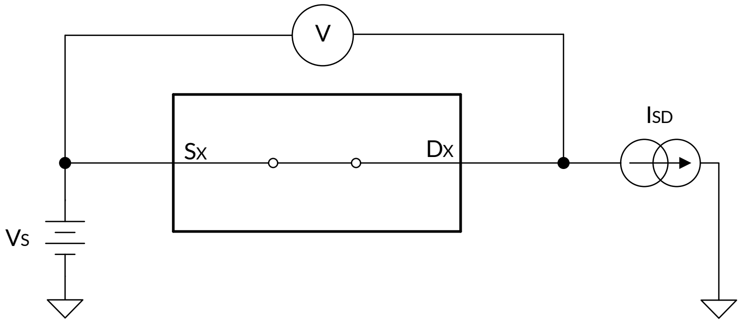


Figure 11. On-Resistance Measurement Setup

8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 12 shows the setup used to measure both off-leakage currents.

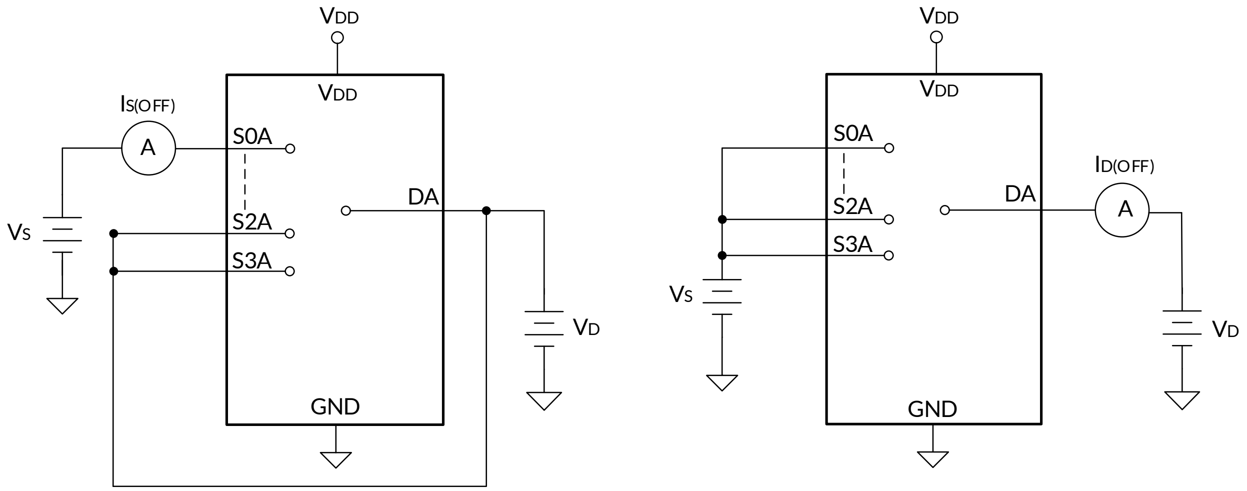


Figure 12. Off-Leakage Measurement Setup

8.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 13 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

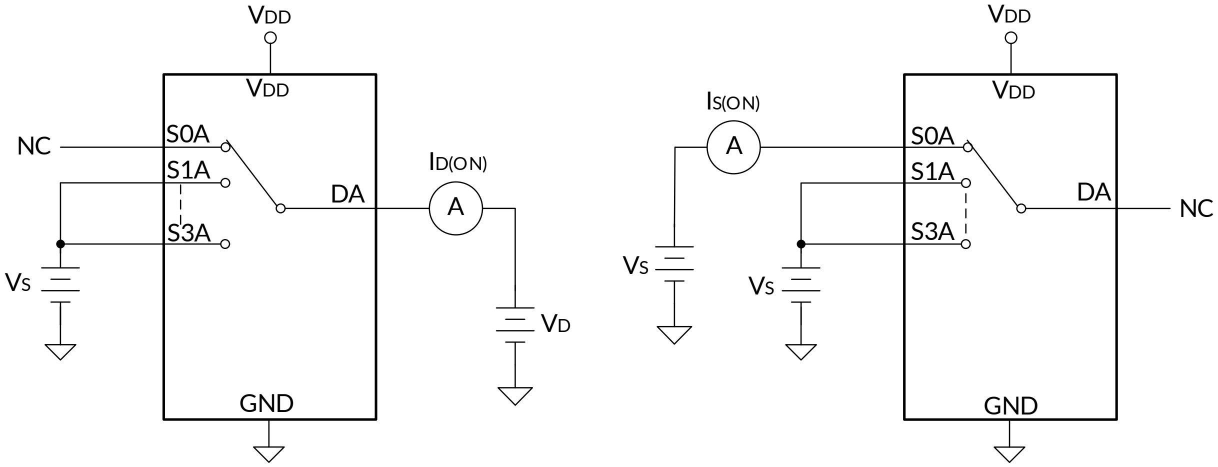


Figure 13. On-Leakage Measurement Setup

8.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 50% after the address signal has risen or fallen past the 50% threshold. Figure 14 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

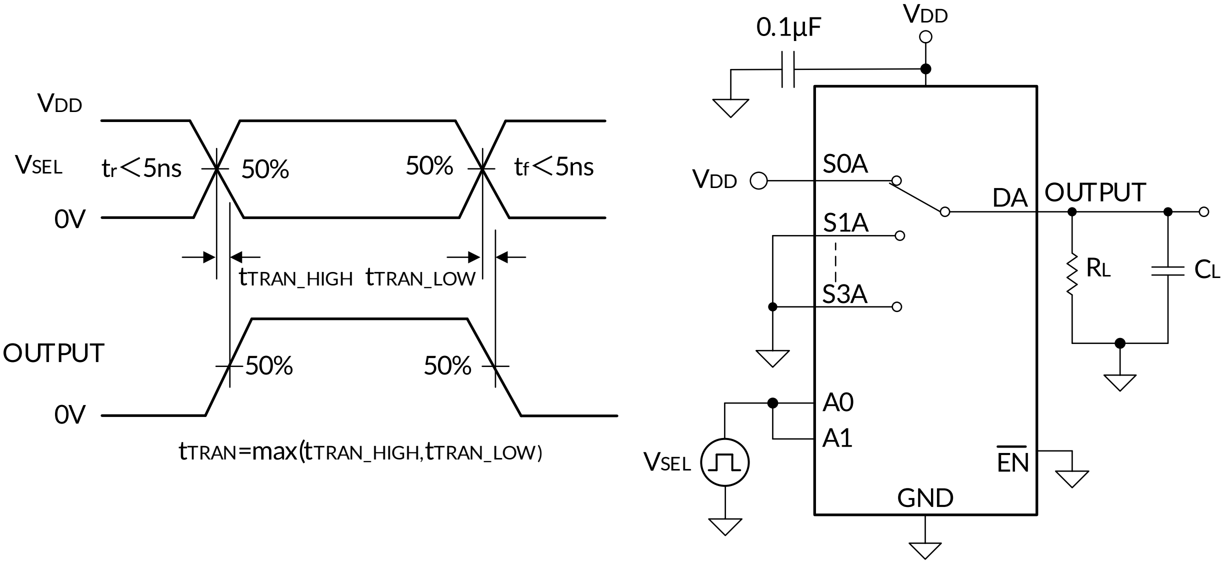


Figure 14. Transition-Time Measurement Setup

8.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as break-before-make delay. Figure 15 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

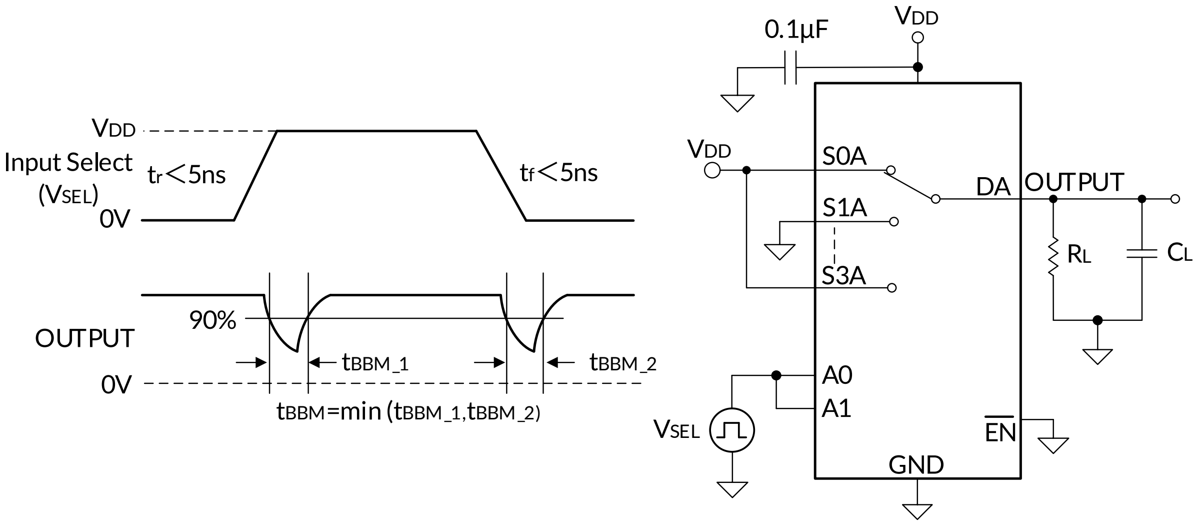


Figure 15. Break-Before-Make Delay Measurement Setup

8.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the 50% threshold. The 10% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 16 shows the setup used to measure transition time, denoted by the symbol $t_{ON(EN)}$.
Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the 50% threshold. The 90% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 16 shows the setup used to measure transition time, denoted by the symbol $t_{OFF(EN)}$.

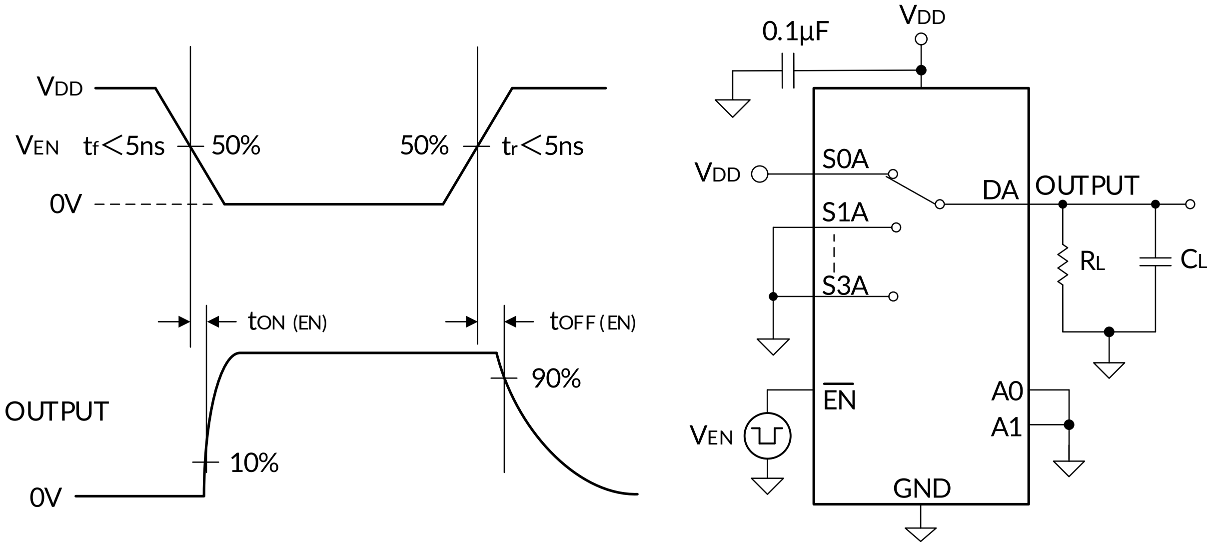


Figure 16. Turn-On and Turn-Off Time Measurement Setup

8.7 Charge Injection

The RMUX1309 device have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol QC. Figure 17 shows the setup used to measure charge injection from source (S_X) to drain (D).

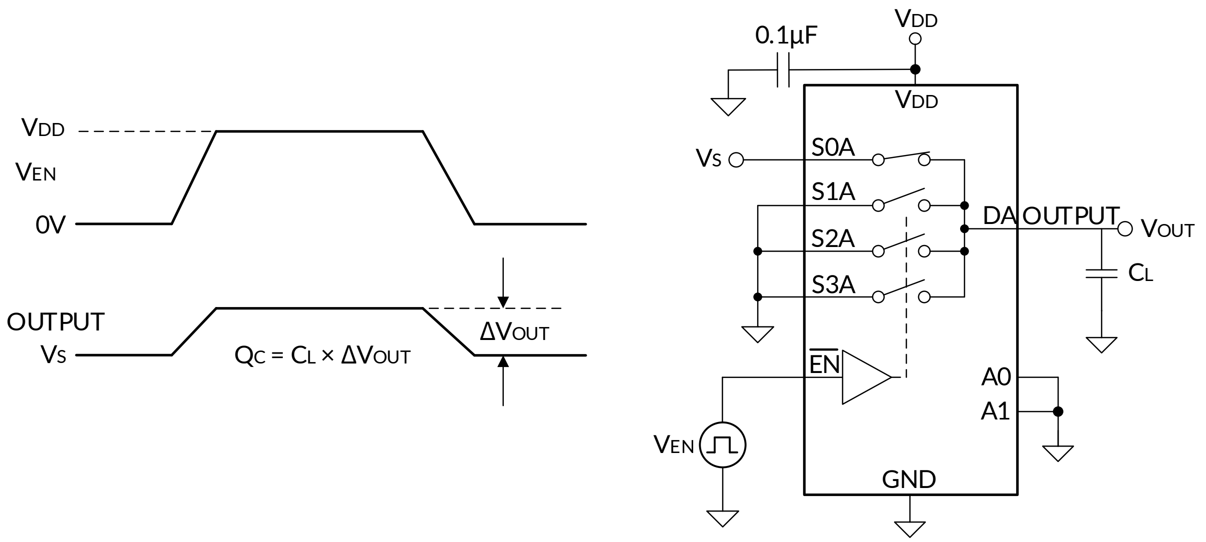


Figure 17. Charge-Injection Measurement Setup

8.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S_X) of an off-channel. Figure 18 shows the setup used to measure, and the equation to compute off isolation.

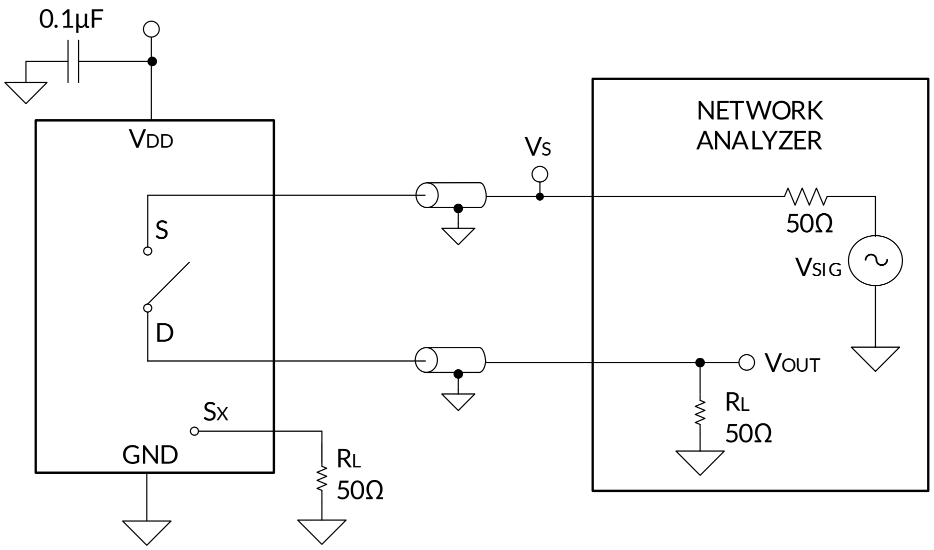


Figure 18. Off Isolation Measurement Setup

$$\text{Off Isolation}=20\bullet\text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

8.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (S_X) of an on-channel. Figure 19 shows the setup used to measure, and the equation used to compute crosstalk.

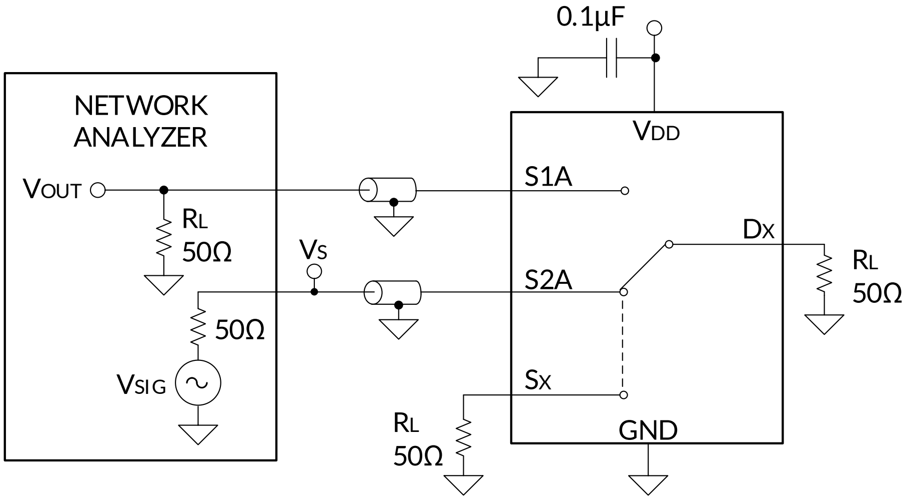


Figure 19. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk}=20\bullet\text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

8.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (S_X) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 20 shows the setup used to measure bandwidth.

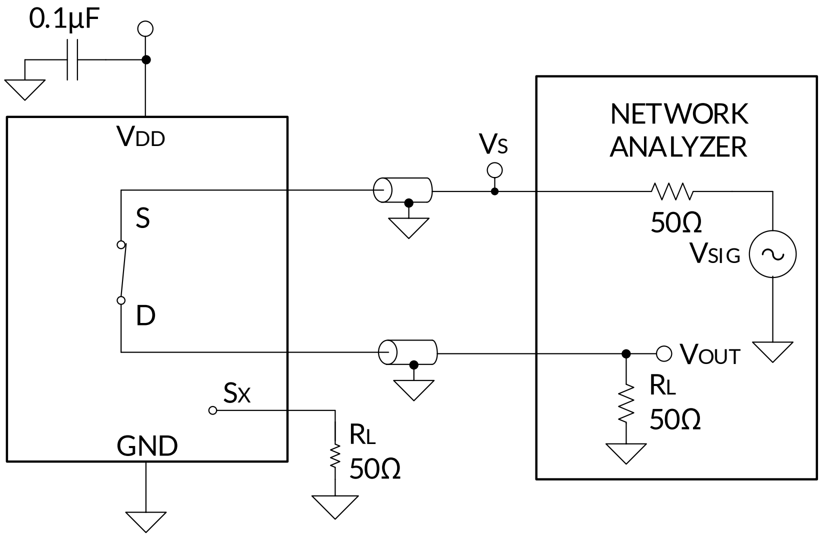


Figure 20. Bandwidth Measurement Setup

$$\text{Attenuation}=20\bullet\text{Log}\left(\frac{V_2}{V_1}\right)$$

8.11 Injection Current Control

Injection current is measured at the change in output of the enabled signal path when a current is injected into a disabled signal path. Figure 21 shows the setup used to measure injection current control.

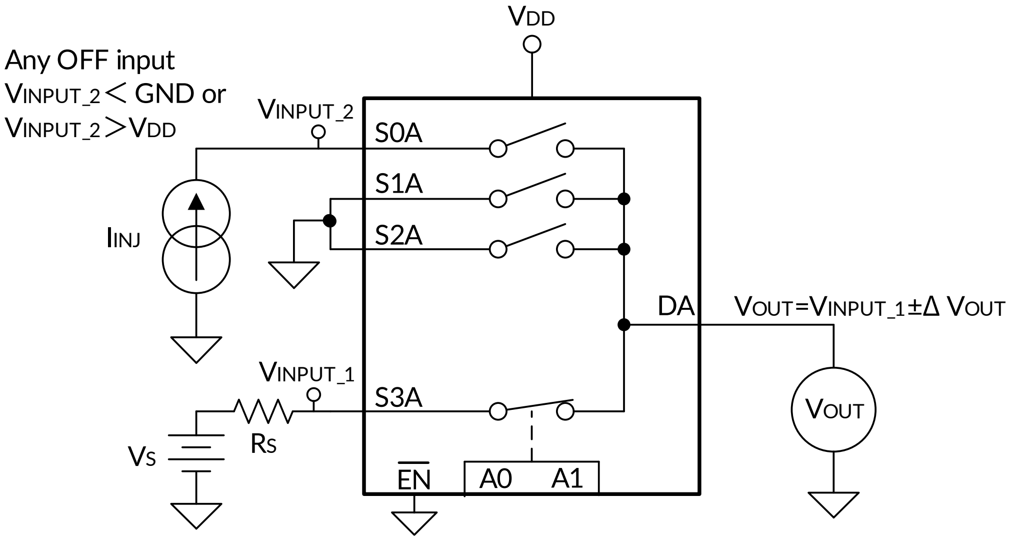


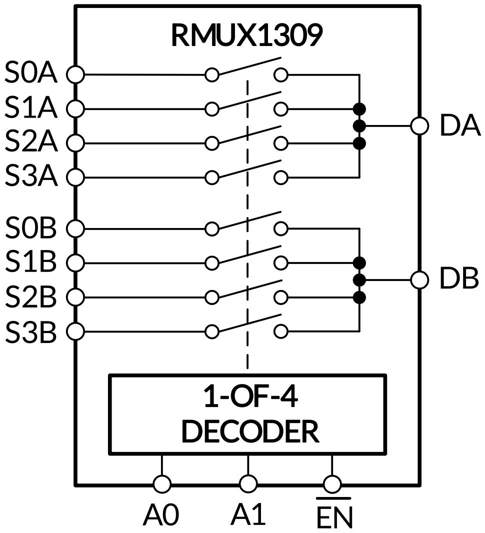
Figure 21. Injection Current Measurement Setup

9 DETAILED DESCRIPTION

9.1 Overview

The RMUX1309 is a 4:1, differential (2- channel) mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bidirectional Operation

The RMUX1309 devices conduct equally well from source (S_X) to drain (D_X) or from drain (D_X) to source (S_X). Each signal path has very similar characteristics in both directions so they can be used as both multiplexers and demultiplexer to support both analog and digital signals.

9.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for the RMUX1309 ranges from GND to V_{DD}.

9.3.3 1.8V Logic Compatible Inputs

The RMUX1309 support 1.8V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails and eliminates the need for an external voltage translator, which saves both space and BOM cost. The current consumption of the RMUX1309 devices increase when using 1.8V logic with higher supply voltage. For more information on 1.8V logic implementations, refer to Simplifying Design with 1.8V logic Muxes and Switches.

9.3.4 Fail-Safe Logic

The RMUX1309 device have Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the RMUX1309 to be ramped to 5.5V while V_{DD} = 0V. Additionally, the feature enables operation of the multiplexers with V_{DD} = 1.8V while allowing the select pins to interface with a logic level of another device up to 5.5V, eliminating the potential need for an external voltage translator.

9.3.5 Injection Current Control

Injection current is the current that is being forced into a pin by an input voltage (V_{IN}) higher than the positive supply (V_{DD} + ΔV) or lower than ground (V_{SS}). The current flows through the input protection diodes into whichever supply of the device is potentially compromising the accuracy and reliability of the system. Injected currents can come from various sources depending on the application.

- Harsh environments and applications with long cabling, such as in factory automation and automotive systems, may be susceptible to injected currents from switching or transient events.
- Other self-contained systems can also be subject to injected current if the input signal is coming from various sensors or current sources.

Injected Current Impact: typical CMOS switches have ESD protection diodes on the inputs and outputs. These diodes not only serve as ESD protection but also provide a voltage clamp to prevent the inputs or outputs going above V_{DD} or below GND and V_{SS}. When current is injected into the pin of a disabled signal path, a small amount of current goes through the ESD diode but most of the current goes through conduction to the drain. If forward diode voltage of the ESD diode (VF) is greater than the PMOS threshold voltage (VT), then the PMOS of all OFF switches turns ON and there would be undesirable subthreshold leakage between the source and the drain that can lift the OFF source pins up also. Figure 22 shows a simplified diagram of a typical CMOS switch and associated injected current path.

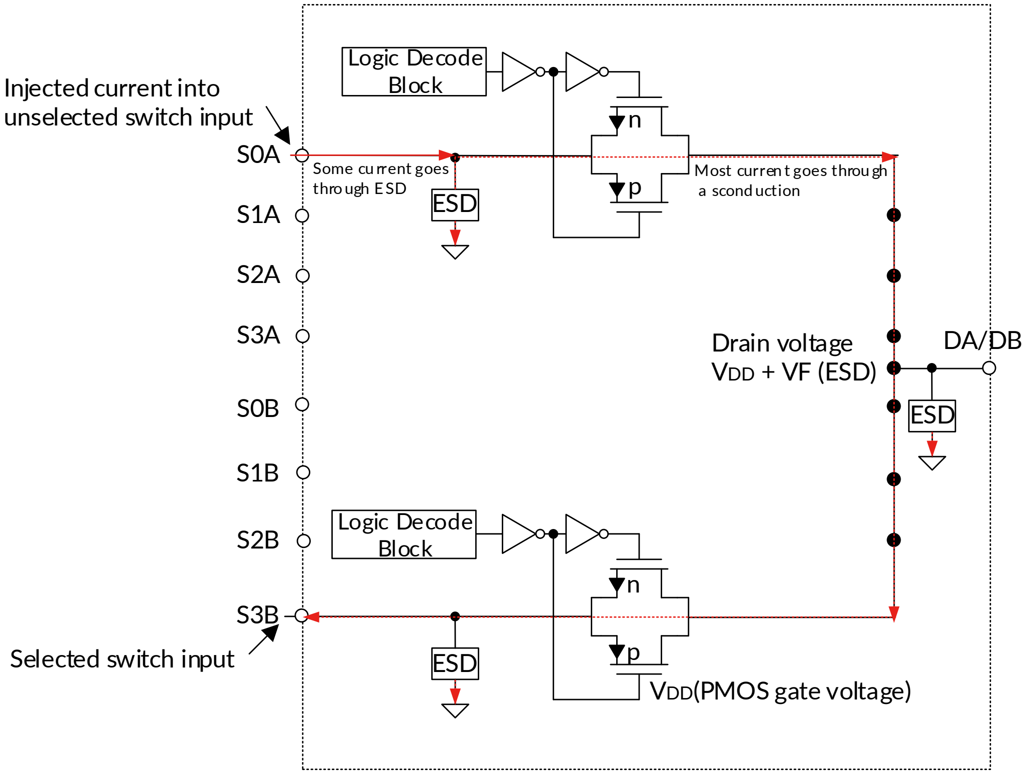


Figure 22. Simplified Diagram of Typical CMOS Switch and Associated Injected Current Path

It is quite difficult to cut off these current paths. The drain pin can never be allowed to exceed the voltage above V_{DD} by more than a VT. Analog pins can be protected against current injection by adding external components like a Schottky diode from the drain pin to ground to clamp the drain voltage at < V_{DD} + VT and cut off the current path.

Change in R_{ON} due to Current Injection: because the ON resistance of the enabled FET switch is impacted by the change in the supply rail, when the drain pin voltage exceeds the supply voltage by more than a VT, an error in the output signal voltage can be expected. This undesired change in the output can cause issues related to false trigger events and incorrect measurement readings, potentially compromising the accuracy and reliability of the system. As shown in Figure 23, S2 is the enabled signal path that is conducting a signal from S2 pin to D pin. Because there is an injected current at the disabled S1 pin, the voltage at that pin increases above the supply voltage and the ESD protection diode is forward biased, shifting the power supply rail. This shift in supply voltage alters the R_{ON} of the internal FET switches, causing a ΔV error on the output at the D pin.

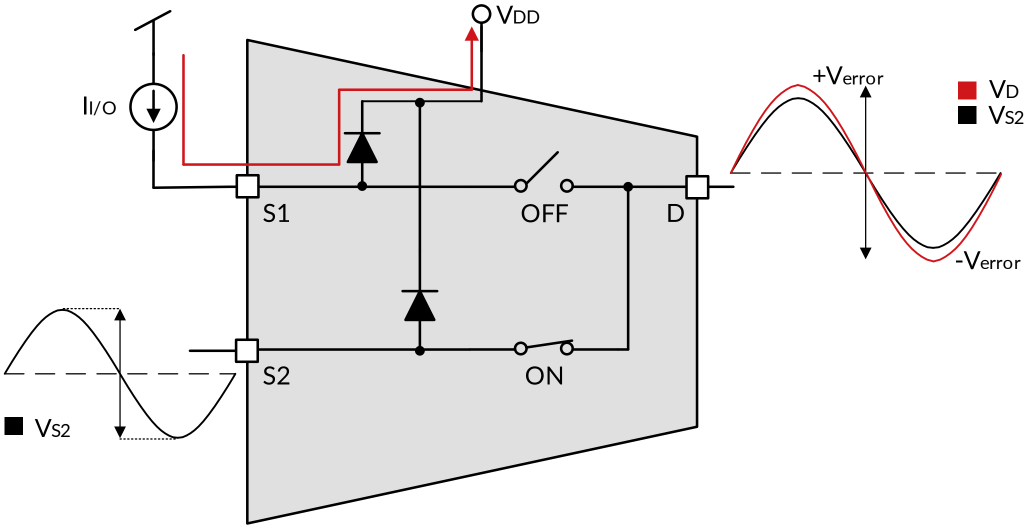


Figure 23. Injected Current Impact on R_{ON}

To avoid the complications of added external protection to your system, the RMUX1309 devices have an internal injection current control feature which eliminates the need for external diode and resistor networks typically used to protect the switch and keep the input signals within the supply voltage. The internal injection current control circuitry allows the signals on the disabled signal paths to exceed the supply voltage without affecting the signal of the enabled signal path. The injection current control circuitry also protects the RMUX1309 from currents injected into disabled signal paths without impacting the enabled signal path, which typical CMOS switches do not support. Additionally, the RMUX1309 do not have any internal diode paths to the supply pin, which eliminates the risk of damaging components connected to the supply pin or providing unintended power to the system supply rail. For a simplified diagram that shows one signal path for the RMUX1309 devices and the associated injection current circuit, refer to Section 9.2.

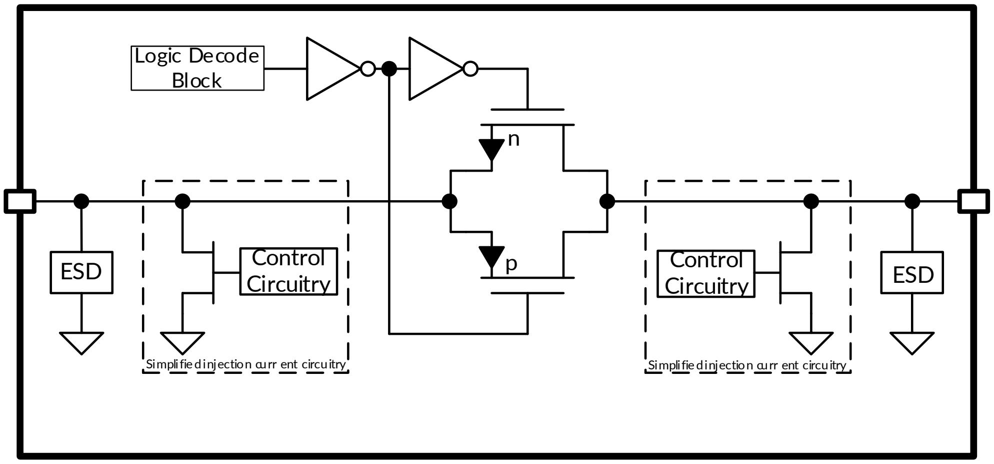


Figure 24. Simplified Diagram of Injection Current Control

The injection current control circuitry is independently controlled for each source or drain pin (S_X or D_X). The control circuitry for a particular pin is enabled when that input is disabled by the logic pins and the injected current causes the voltage at the pin to be above V_{DD} or below GND. The injection current circuit includes an FET to shunt the undesired current to GND in the case of overvoltage or injected current events. Each injection current circuit is rated to handle up to 50 mA; the device, however, can support a maximum current of 100 mA at any given time. Depending on the system application, a series limiting resistor may be needed and must be sized appropriately. Figure 24 shows the RMUX1309 protection circuitry with an injected current at an input pin.

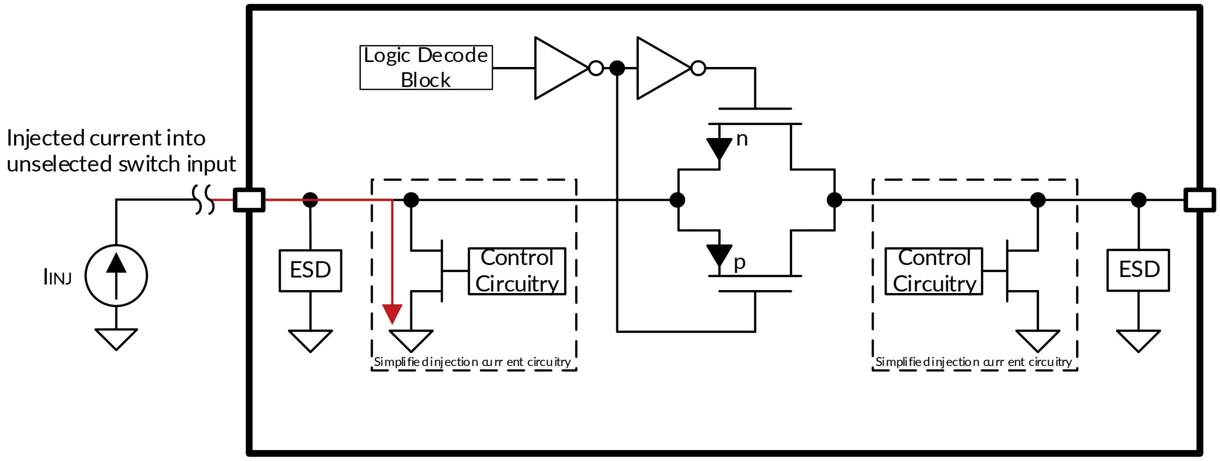


Figure 25. Injected Current at Input Pin

Figure 26 shows an example of using a series limiting resistor in the case of an over-voltage event.

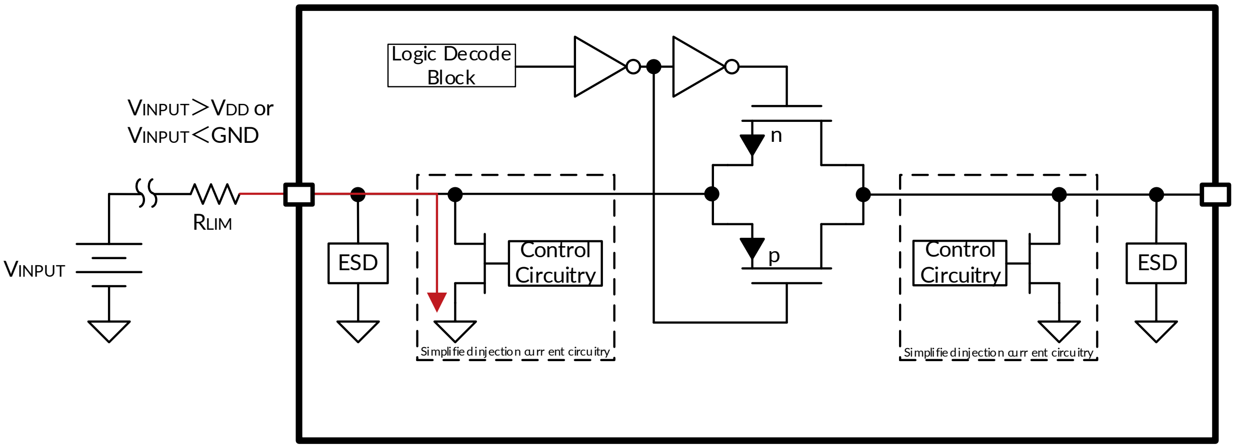


Figure 26. Over-Voltage Event with Series Resistor

For the injection current control circuitry to be active, two conditions must be present. First, the voltage at the source or drain pins is greater than V_{DD}, or less than GND. Next, the channel must be unselected. With those two requirements met, the protection FET will be turned on for any disabled signal path and shunt the pin to GND. In this event, a series resistor is needed to limit the total current injected into the device to be less than 100 mA. Three example scenarios are outlined in the following sections.

9.3.5.1 RMUX1309 is Powered, Channel is Unselected, and the Input Signal is Greater Than V_{DD} (V_{DD} = 5V, V_{INPUT} = 5.5V)

A typical CMOS switch would have an internal ESD diode to the supply pin rated for ≅30 mA that would be turned on and a series limited resistor would be needed. However, any conducted current would be injected into the supply rail potentially damaging the system, unexpectedly turning on other devices on the same supply rail, or requiring additional components for protection. The RMUX1309 implementation also handles this scenario with a series limiting resistor; the current path, however, is now to GND which does not have the same issues as the current injected into the supply rail.

9.3.5.2 RMUX1309 is Powered, Channel is Selected, and the Input Signal is Greater Than V_{DD} (V_{DD} = 5V, V_{INPUT} = 5.5V)

The injection current control circuitry is fully active when the channel is unselected and an overvoltage event is present (overvoltage being defined as 0.5 V above the supply rail). However, in situations where the channel is selected and an overvoltage event occurs, this protection circuitry will still be partially active. In this instance, a portion of the injected current will be redirected through the protection circuitry to GND, but will not be a full shunt. So, some current will also flow through the source to drain path. This allows the device to tolerate overvoltage conditions in the event of the channel being selected, but precautions are still necessary to protect the device from overcurrent events such as implementing a current limiting resistor to keep the device below the maximum continuous source and drain current specification.

9.3.5.3 RMUX1309 is Unpowered and the Input Signal has a Voltage Present (V_{DD} = 0 V, V_{INPUT} = 3 V)

Many CMOS switches are unable to support a voltage at the input without a valid supply voltage present, otherwise the voltage will be coupled from input to output and could damage downstream devices or impact power-sequencing. The RMUX1309 circuitry can handle an input signal present without a supply voltage while minimizing power transfer from the input to output of the switch. By limiting the output voltage coupling to 400mV the RMUX1309 help reduce the chance of conduction through any downstream ESD diodes.

9.4 Device Functional Modes

When the $\overline{\text{EN}}$ pin of the RMUX1309 is pulled low, one of the switches is closed based on the state of the address lines. Similarly, when the $\overline{\text{EN}}$ pin of the RMUX1309 is pulled low, two of the switches are closed based on the state of the address lines. When the $\overline{\text{EN}}$ pin is pulled high, all the switches are in an open state regardless of the state of the address lines.

Unused logic control pins must be tied to GND or V_{DD} to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (S_X and D_X) should be connected to GND.

9.5 Truth Tables

Table 1 provides the truth tables for the RMUX1309 respectively.

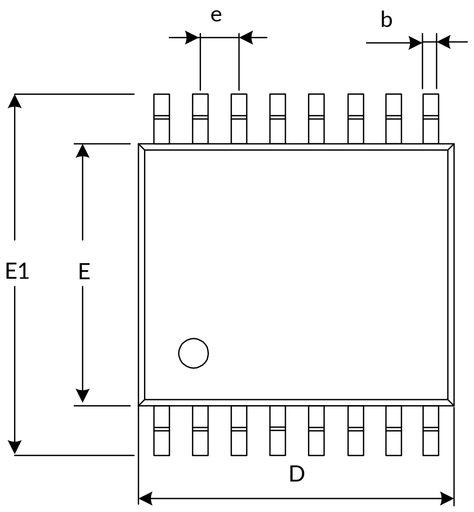
Table 1. RMUX1309 Truth Table

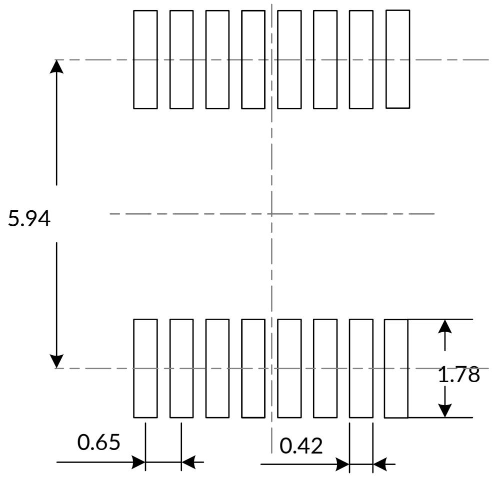
$\overline{\text{EN}}$	A1	A0	Selected Signal Path Connected to Drain (DA and DB) Pins
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X (1)	X (1)	All channels are off

(1) X denotes do not care.

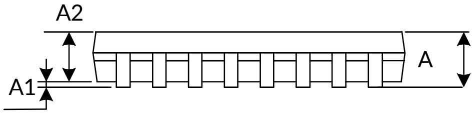
10 PACKAGE OUTLINE DIMENSIONS

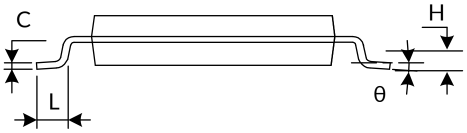
TSSOP16 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



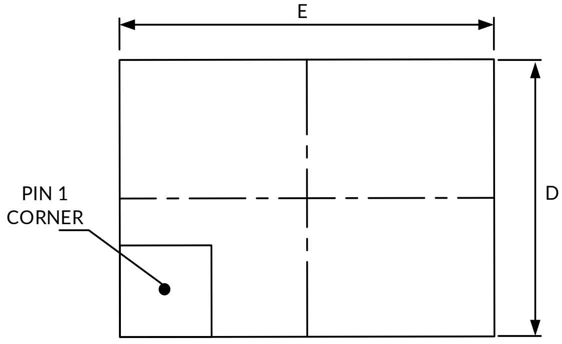


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.02	0.028
H	0.25TYP		0.01TYP	
θ	1°	7°	1°	7°

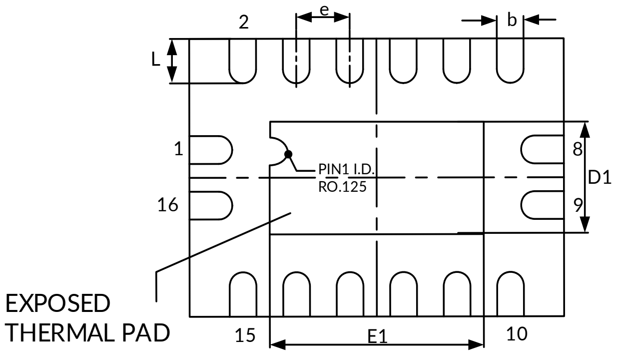
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

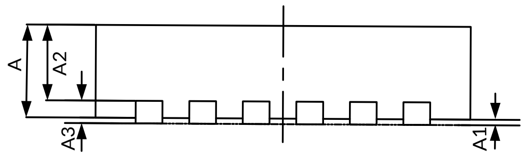
QFN2.5X3.5-16 (4)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A2	0.600	0.700	0.024	0.028
A3	0.203(REF) (2)		0.008(REF) (2)	
D (1)	2.400	2.600	0.094	0.102
E (1)	3.400	3.600	0.134	0.142
e	0.500(BSC) (3)		0.020(BSC) (3)	
b	0.180	0.300	0.007	0.012
L	0.300	0.500	0.012	0.020
D1	0.850	1.150	0.033	0.045
E1	1.850	2.150	0.073	0.085

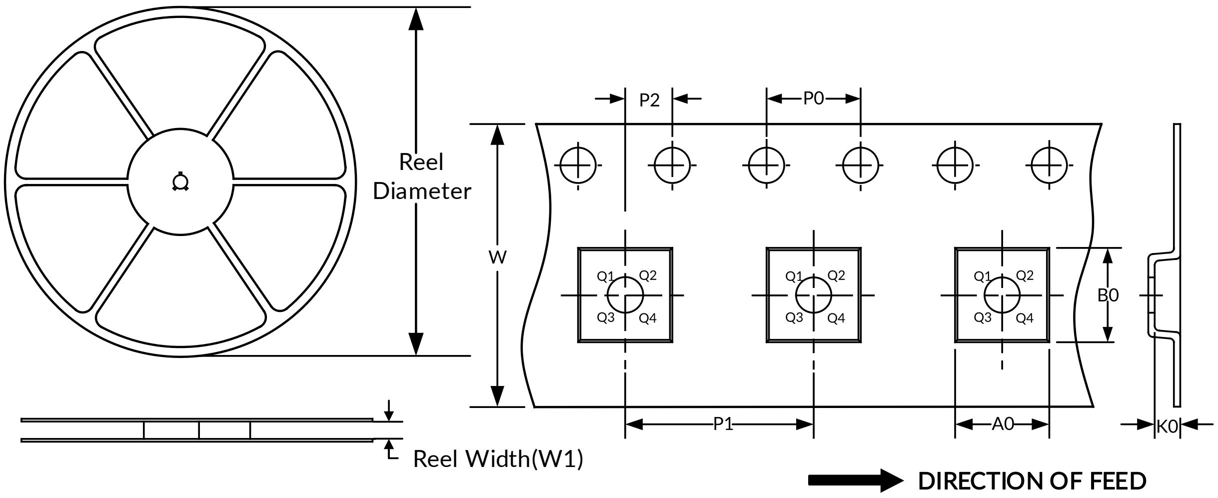
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP16	13”	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1
QFN2.5X3.5-16	7”	15.0	2.80	3.80	1.20	4.0	4.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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